ARMY
NAVY
AIR FORCE

TM 11-6625-3025-14
ET426-AA-MMA-010/E154 VII210
T.O. 33A1-8-902-1-1

TECHNICAL MANUAL

OPERATOR'S, ORGANIZATIONAL, DIRECT SUPPORT AND GENERAL SUPPORT MAINTENACE MANUAL FOR

GENERATOR, TEST PATTERN SG-1 223/T (NSN 6625-01-127-6846)

DEPARTMENTS OF THE ARMY, NAVY, AND AIR FORCE

10 JANUARY 1983

5 SAFETY STEPS TO FOLLOW IF SOMEONE IS THE VICTIM OF ELECTRICAL SHOCK

1 DO NOT TRY TO PULL OR GRAB THE INDIVIDUAL

2 IF POSSIBLE, TURN OFF THE ELECTRICAL POWER

3 IF YOU CANNOT TURN OFF THE ELECTRICAL POWER, PULL, PUSH, OR LIFT THE PERSON TO SAFETY USING A DRY WOODEN POLE OR A DRY ROPE OR SOME OTHER INSULATING MATERIAL

4 SEND FOR HELP AS SOON AS POSSIBLE

5 AFTER THE INJURED PERSON IS FREE OF CONTACT WITH THE SOURCE OF ELECTRICAL SHOCK, MOVE THE PERSON A SHORT DISTANCE AWAY AND IMMEDIATELY START ARTIFICIAL RESUSCITATION

WARNING

USE OF CLEANING SOLVENT

Fumes of TRICHLOROTRIFUOROETHANE are poisonous. Provide adequate ventilation whenever you use TRICHLOROTRIFLUOROETHANE. Do not use solvent near heat or open flame. TRICHLOROTRIFLUOROETHANE will not burn, but heat changes the gas into poisonous, irritating fumes. DO NOT breathe the fumes or vapors. TRICHLOROTRIFUOROETHANE dissolves natural skin oils. DO NOT get the solvent on your skin. Use gloves, sleeves and an apron which the solvent cannot penetrate. If the solvent is taken internally, see a doctor immediately.

WARNING

HIGH VOLTAGES

High voltage is used in this equipment. Be careful when working near the interior of the equipment, or near the ac power distribution. Observe warning notes in this technical manual and warning decals on equipment. Death on contact may result if safety precautions are not observed.

WARNING

Compressed air shall not be used for cleaning purposes except where reduced to less than 29 pounds per square inch (psi) and then only with effective chip guarding and personnel protective equipment. Do not use compressed air to dry parts when TRICHLOROTRIFLUOROETHANE has been used. Compressed air is dangerous and can cause serious bodily harm if protective means or methods are not observed to prevent chip or particle (of whatever size) from being blown into the eyes or unbroken skin of the operator or other personnel.

TECHNICAL MANUAL
NO. 11-6625-3025-14
TECHNICAL MANUAL
EE426-AA-MMA-010/E154 VII210
TECHNICAL ORDER
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T.O. 33A1-8-902-1-1

DEPARTMENTS OF THE ARMY

THE NAVY, AND THE AIR FORCE

WASHINGTON, DC 10 JANUARY 1983

OPERATOR'S, ORGANIZATIONAL,

DIRECT SUPPORT, AND GENERAL SUPPORT

MAINTENANCE MANUAL

FOR

GENERATOR, TEST PATTERN

SG-1223/T

(NSN 6625-01-127-6846)

REPORTING ERRORS AND RECOMMENDING IMPROVEMENTS

You can help improve this manual. If you find any mistakes or if you know of a way to improve the procedures, please let us know. Mail your letter, DA Form 2028 (Recommended Changes to Publications and Blank Forms), or DA Form 2028-2 located in back of this manual direct to: Commander, US Army Communications - Electronics Command and Fort Monmouth, ATTN: DRSEL-ME-MP, Fort Monmouth, New Jersey 07703.

For Air Force, submit AFTO Form 22 (Technical Order System Publication Improvement Report and Reply) in accordance with paragraph 6-5, Section VI, T.O. 00-5-1. Forward direct to prime ALC/MST. For Navy, mail comments to the Commander, Naval Electronics Systems Command, ATTN: ELEX 8122, Washington, DC 20360.

In either case, a reply will be furnished direct to you.

This manual is an authentication of the manufacturer's commercial literature which, through usage, has been found to cover the data required to operate and maintain this equipment. Since the manual was not prepared in accordance with military specifications and AR 310-3, the format has not been structured to consider levels of maintenance.

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CHAPTER 1

INTRODUCTION

Section I. GENERAL

1-1. Scope. This manual describes the Generator, Test Pattern SG-1223/T (figure 1-1), hereafter referred to as the test pattern generator. The manual contains information on the functioning of equipment, installation, and operation. The manual also provides organizational and general support maintenance instructions, including troubleshooting, repair and adjustments. A complete listing of reference publications is provided in Appendix A. The Maintenance Allocation Chart is contained in Appendix B. The Repair Parts and Special Tools List (RPSTL) is contained in TM 11-6625-3025-24P.

1-2. Consolidated Index of Army Publications and Blank Forms.

a. Army. Refer to the latest issue of DA Pam 310-1 to determine whether there are new editions, changes, or additional publications pertaining to the equipment.

b. Air Force. Use T.O. 0-1-31 Series Numerical Index and Requirements Table (NIRT).

1-3. Maintenance Forms, Records and Reports.

a. Reports of Maintenance and Unsatisfactory Equipment. Department of the Army forms and procedures used for equipment maintenance will be those prescribed by TM 38-750, The Army Maintenance Management System (Army). Air Force personnel will use AFR 66-1 for maintenance reporting and TO-00-35D54 for unsatisfactory equipment reporting. Navy personnel will report maintenance performed utilizing the Maintenance Data Collection Subsystem (MDCS) IAW OPNAVINST 4790.2, Vol 3, and unsatisfactory material/conditions (UR submissions) IAW OPNAVINST 4790.2, Vol 2, chapter 17.

b. Report of Packaging and Handling Deficiencies. Fill out and forward SF 364 (Report of Discrepancy (ROD)) as prescribed in AR 735-11-2/DLAR 4140.55/NAVMATINST 4355.73/AFR 400-54/MCO 4430.3E.

c. Discrepancy in Shipment Report (DISREP) (SF 361). Fill out and forward Discrepancy in Shipment Report (DISREP) (SF 361) as prescribed in AR 55-38/NAVSUPINST 4610.33B/AFR 75-18/MCO P4610.19C/DLAR 4500.15.

1-4. Reporting Equipment Improvement Recommendations (EIR).

a. Army. If your Test Pattern Generator SG-1223/T needs improvement, let us know. Send us an EIR. You, the user, are the only one who can tell us what you don't like about your equipment. Let us know why you don't like the design. Put it on an SF 368 (Quality Deficiency Report). Mail it to Commander, US Army Communications-Electronics Command and Fort Monmouth, ATTN: DRSEL-ME-MP, Fort Monmouth, New Jersey 07703. We'll send you a reply.

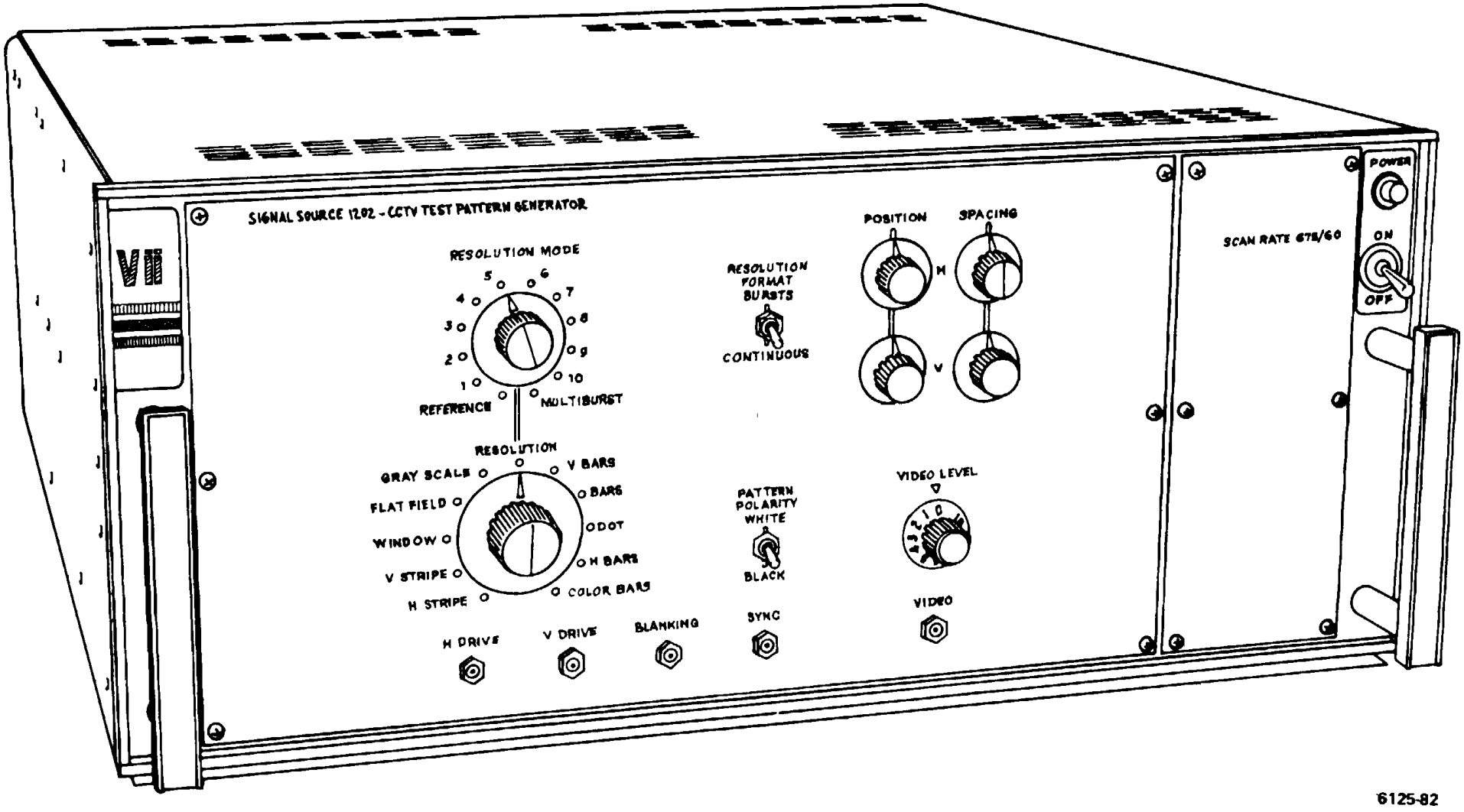


Figure 1-1. Generator, Test Pattern SG-1223/T

b. Air Force. Air Force personnel are encouraged to submit EIR's in accordance with AFM 900-4.

c. Navy. Navy personnel are encouraged to submit EIR's through their local Beneficial Suggestion Program.

1-5. Administrative Storage. Administrative Storage of equipment issued to and used by Army activities will have maintenance performed in accordance with Chapter 5, before storing. When removing the equipment from administrative storage, routine checks (paragraph 5-3) should be performed to assure operational readiness.

1-6. Destruction of Army Electronics Materiel. Destruction of Army electronics materiel to prevent enemy use shall be in accordance with TM 750-244-2.

Section II. DESCRIPTION AND DATA

1-7. Purpose and Use. The Test Pattern Generator SG-1223/T provides a basic set of video test patterns required to align, adjust, troubleshoot, and verify repair of video display monitoring equipment.

1-8. Description. The test pattern generator is a portable, self-contained instrument that provides the composite video signal which contains vertical and horizontal sync information, blanking and pattern information necessary to evaluate the performance of video display equipment.

The basic chassis is composed of a vertical card file which contains the replaceable, plug-in power regulator and pattern development circuit cards. Removing the top panel provides access to the plug-in circuit cards. The front panel assembly includes all controls for operating the test pattern generator. Power and signals connections are made at the rear of the case. Operating power is supplied by power regulators mounted on a heat sink attached to the rear panel. Vent openings on the top panel allow cooling air to circulate through the interior of the unit.

1-9. Technical Characteristics.

a. Sync Generator Section.

(1) Output signals (one each of the following pulses):

Type	H drive, V drive, blanking, sync
Level	4v peak
Polarity	Negative-going pulses
Impedance	75 ohm source termination
Risetime	Nominally 0.1 usec
Coupling	AC (capacitive)

(2) Input signal requirements: None

(3) Controls:

External	None
Internal	H front porch
	H sync width
	H blanking width
	H drive width
	Pulse amplitude

(4) Scan rates: 2:1 interlace, at 675/60 scan rate

Rate	
Lines per frame	675
Lines per field	337.5
Field rate	60
2H master oscillator	40.500 KHz
H rep rate	20.250 KHz
Total H line	49.4 usec
Active H line	42.4 usec

(5) Waveform: Circuit card jumper selection of Industrial waveform in accordance with EIA Standard RS-343.

Typical pulse widths

V drive	13.5 lines
V drive porch	3 lines
V sync	3 lines
V post	3 lines
V blanking	26 lines
H blanking	7.0 usec
H drive	3.5 usec
H front porch	1.0 usec
H sync	2.75 usec
2H equalizing	1.4 usec
2H serrations	2.0 usec

b. Pattern Generator Section.

(1) Functions:

Flat field	Uniform white level over entire active area.
V stripe	Nominally 50% of each scan line at white level, 50% at black level, for test of transient and mid-frequency response.
H stripe	Nominally 50% of the vertical field at white level, 50% at black level, for test of low frequency response at field rate.
Window	A 25% duty cycle test, combination of H stripe and V stripe, for combined transient and low frequency response tests.
Gray scale	Standard ten step slope adjustable to linear or log.
V bars	Straight vertical lines accurately spaced to serve as a linearity reference in the horizontal plane of a video display.
H bars	Straight horizontal lines accurately spaced to serve as a linearity reference in the vertical plane of a video display.
Bars	A combination of the H bars and V bars to form a grid ("crosshatch" or "grating") for linearity reference in both display planes simultaneously.

Dots	Small pin points developed at the intersection of the H bar and V bar elements, especially for linearity measurements with the EIR linearity (ball) chart.
Resolution	Square wave bar pattern at selected repetition rate to develop desired resolution tv lines in ten increments (usually 100 to 1000 lines at 100-line steps), at full, 100% black-to-white contrast. Presented as continuous, burst or multiburst. Reference bars are also selected over entire tv field.

(2) Operating Modes:

Pattern polarity	Selection of either white-on-black or black-on-white patterns for bar, dot, window and related functions.
Calibration	Internal preset calibration for automatic selection of pattern proportion for the 675/60 scan rate. Variable front panel adjustment for certain patterns.

(3) Input signals: None

(4) Output signals:

Type	Composite video	
Level	Video	0 to 1v pk to pk as adjusted by front panel control
	Blanking	Pedestal level adjustable, 0 to 0.15v pk to pk by internal control
	Sync	Level adjustable, 0 to 0.4v pk to pk by internal control
Impedance	75 ohm, source terminated	
Coupling	Direct coupled (dc)	
Polarity	White positive, sync negative	
Connector	BNC type coaxial	

(5) Power requirement:

Voltage	120v (105 to 135v) ac 220v (200 to 270v) ac 240v (200 to 270v) ac
Current	3/4 amp

Power	70 watts
Frequency	50 to 400 Hz
Fuse rating	2.0 amp SLO-BLO

(6) Environmental:

Temperature	0° to +55°C ambient, free air circulation
Humidity	Up to 95%

(7) Enclosure:

Type	Metal cabinet, fully enclosed
Size	7"h x 17"w x 20"d (18cm h x 43cm w x 41cm d)
Weight	Approximately 36 lbs (15 kg)

CHAPTER 2

SERVICE UPON RECEIPT AND INSTALLATION

Section I. SERVICE UPON RECEIPT OF MATERIAL

2-1. Unpacking. No special instructions are required for unpacking the test pattern generator. Remove the instrument from its shipping container and perform the inspection given in paragraph 2-2.

2-2. Checking Unpacked Equipment.

a. Inspect the equipment for damage incurred during shipment. If equipment has been damaged, report the damage on SF 364 (see paragraph 1-3b.) .

b. Check the equipment against the component listing on the packing slip to see if the shipment is complete. Report all discrepancies in accordance with paragraph 1-3c. The equipment should be placed in service even though a minor assembly or part that does not affect proper functioning is missing.

c. Check to see whether the equipment has been modified. Equipment which has been modified will have the MWO number on the front panel near the nomenclature plate. Check also to see whether all currently applicable MWOs have been applied.

Section II. INSTALLATION

2-3. Introduction. The test pattern generator is a portable, self-contained instrument which does not require permanent installation. The unit is ready for installation after unpacking as described in paragraph 2-1. No special tools are required for installation.

2-4. Electrical Interconnection. Perform electrical interconnection as follows:

a. Refer to figures 2-1 and 2-2 and connect the test pattern generator as shown in a typical installation test set-up for a television display device.

b. Check that ac power switch on test pattern generator is in the OFF position.

c. Connect ac power cable of test pattern generator to a 115 VAC, 50-400 Hz power source.

NOTE

Since an internal sync generator is used, no inputs are required and the rear panel connectors can serve as auxiliary sync outputs for external use. If pulse signals are not used elsewhere, terminations (75 ohms) should be installed on each output to permit all signals to be at the proper levels and characteristic impedance.

d. Perform the operating instructions described in Chapter 3.

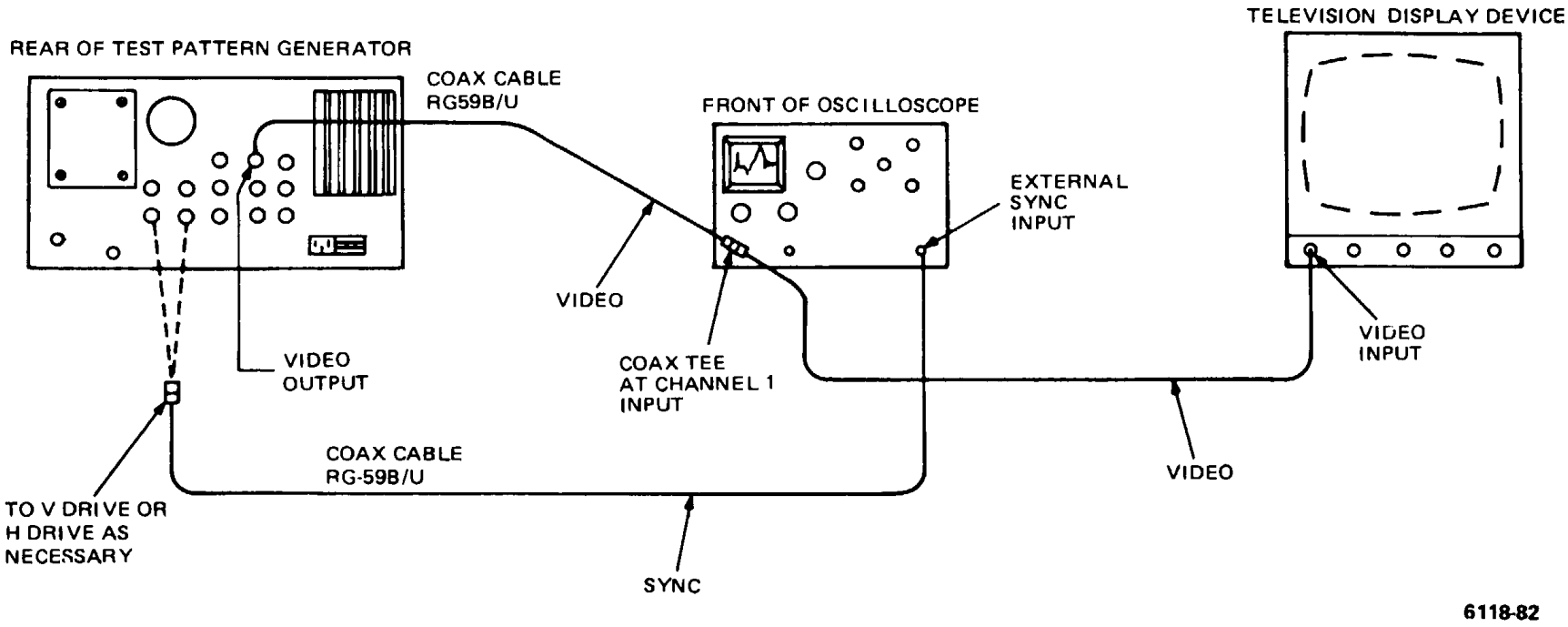


Figure 2-1. Typical Test Setup

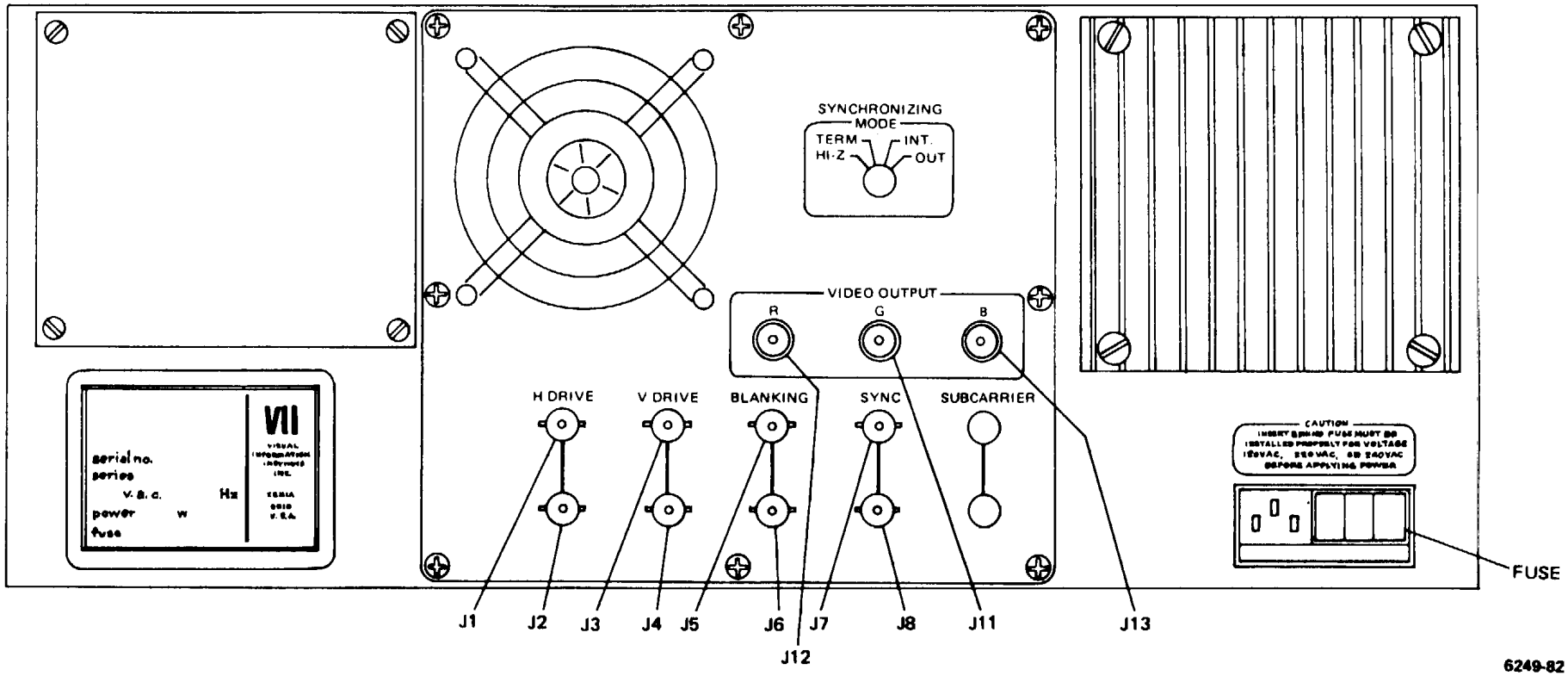


Figure 2-2. Test Pattern Generator, Rear Panel

CHAPTER 3

OPERATING INSTRUCTIONS

Section I. CONTROLS AND INDICATORS

3-1. Introduction. This section describes the operating instructions for the test pattern generator and includes the function of all operating controls and indicators.

3-2. Operator Controls. Controls and indicators used by operating personnel are illustrated in figure 3-1 and described in table 3-1.

3-3. Operating Procedure. Operating procedures for the test pattern generator assume installation has been performed and is ready for use as described in Chapter 2, Section II. The following is a general operating procedure intended to inform the operator of the method of operating the test pattern generator.

a. Turn power switch to the ON position. The red indicator lamp should illuminate and the unit is ready for operation.

b. Select RESOLUTION MODE.

c. Select RESOLUTION format.

d. Select either white-on-black or black-on-white patterns.

e. Adjust desired VIDEO LEVEL.

f. Adjust for desired POSITION and SPACING for appropriate patterns.

The operating procedure will vary according to the user's requirements. Perform the operating procedure in accordance with the instructions outlined in the manual of the display device under test. Refer to paragraph 1-9 (this manual) which defines the operating characteristics of this instrument.

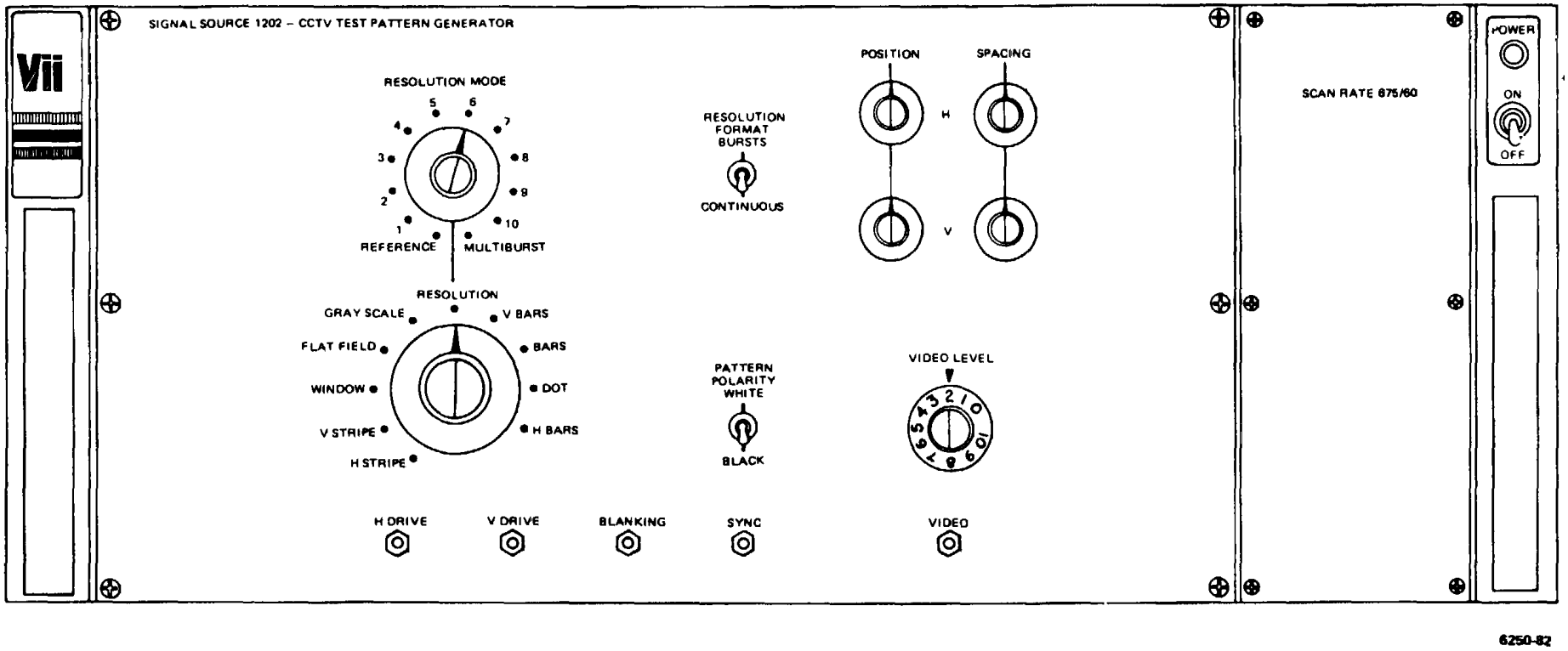


Figure 3-1. Test Pattern Generator, Controls and Indicators

Table 3-1. Test Pattern Generator, Controls and Indicators

Control/indicator	Function
Function select (rotary)	Selector switch which permits the operator to choose the following functions developed in the video output signal:
H STRIPE	Nominally 50% of the vertical field at white level, 50% at black level for test of low frequency response at field rate.
V STRIPE	Nominally 50% of each tv line at white level, 50% at black level, for test of transient and mid-frequency response.
WINDOW	A 25% duty cycle test, combination of H STRIPE and V STRIPE, for combined transient and low frequency response tests.
FLAT FIELD	Uniform white level over entire active area.
GRAY SCALE	Standard ten step slope adjustable to linear or log.
RESOLUTION	Square wave bar pattern at selected repetition rate to develop desired "resolution tv lines", in the ten increments (usually 100 to 1000 tv lines at 100 line steps), at full, 100% black-to-white contrast. Presented as continuous, burst or multiburst. Reference bars also selectable over entire tv field.
V BARS	Straight vertical lines accurately spaced to serve as a linearity reference in the horizontal display plane.
BARS	A combination of the H BARS and V BARS to form a grid ("crosshatch" or "grating") for linearity reference in both display planes simultaneously.
DOTS	Small pin points developed at the intersection of the H BAR and V BAR elements, especially for linearity measurements with the EIA linearity (ball) chart.
H BARS	Straight horizontal lines accurately spaced to serve as a linearity reference in the vertical display plane.

Table 3-1. Test Pattern Generator, Controls and Indicators - Continued

Control/indicator	Function
RESOLUTION Selector (rotary)	When main function selector is in the RESOLUTION position, this switch permits selection of RESOLUTION repetition rate that is in use.
RESOLUTION format (toggle)	Selects either CONTINUOUS or BURSTS resolution pattern, not operable in REFERENCE position.
PATTERN POLARITY (toggle)	Selects either WHITE-on-BLACK or BLACK-on-WHITE patterns for BAR, DOT,WINDOW, and related functions.
H SPACING	Adjusts the width between pattern elements in the horizontal dimension of the television display, selecting the number of H elements which will be displayed for the BAR, DOT, H BAR and V BAR patterns.
V SPACING	Adjusts the width between pattern elements in the vertical dimension of the television display, and therefore controls the number of V elements which will be displayed for the BAR, DOT, H BAR and V BAR patterns.
H POSITION	Controls the position of the pattern in the horizontal dimension of the television raster for appropriate patterns.
V POSITION	Controls position of the pattern in the vertical dimension of the television raster for appropriate patterns.
VIDEO LEVEL	Controls the amplitude of video portion of the composite signal which is presented at the output.
POWER ON/OFF switch (toggle)	Applies 115 VAC, 50 - 400 Hz to test pattern generator in the ON position. generator in the ON position.
AC power on indicator (red)	Illuminates when 115 volts, 50 - 400 Hz is (red) applied to power supply circuit
Test points	To verify presence of proper H DRIVE, V DRIVE, BLANKING, SYNC and VIDEO output signals at the inputs and outputs.

CHAPTER 4

FUNCTIONING OF EQUIPMENT

Section I. OVERALL FUNCTIONAL DESCRIPTION

4-1. Introduction. This chapter provides a functional description of the test pattern generator. The functional description is presented in two levels. Section I contains a brief overall functional description of the circuit cards shown in the test pattern generator functional block diagram, figure FO-2, and section II contains a more detailed description of the individual circuit card function based on fold-out schematic diagrams in each functional area.

4-2. Sync Generation. (See figure FO-2). The synchronizing ("sync") generator produces pulses which are used to synchronize camera, display monitor and other television devices in developing the tv raster. These pulses control the order in which the television picture will be produced. Four basic types of electrical pulse signals have become commonly used for such purposes, including H drive, V drive, blanking and sync (see figure 4-1), as described by Electronic Industries Association (EIA) Standard RS-343. All pulses are generated from a very stable master oscillator which is crystal controlled. Digital techniques are used to generate pulses at the horizontal and vertical rates of the scan rate to be used. These include:

a. H DRIVE is a pulse train in which a pulse starts at the end of every television scanning line. Its function is to mark the time interval between the end of one line and the start of another; the pulses may be used to control horizontal deflection "flyback" and signal processing. The pulse train is continuous, uninterrupted even during the vertical synchronizing interval. These pulses are useful for synchronizing an oscilloscope when inspecting the television waveform at the horizontal line rate.

b. V DRIVE is a pulse train in which a pulse starts at the end of each television field. Its function is to mark the time interval between the end of one television field and the next; these pulses may be used to control vertical deflection "flyback" and signal processing. These pulses are useful for synchronizing an oscilloscope when inspecting the television waveform at vertical field rate.

c. BLANKING is a mixture of horizontal and vertical information intended to control the "blackout" of the television system during deflection return between horizontal lines and vertical fields. These pulses are wider than drives or sync to insure that all transitions are made invisible.

d. SYNC is a complex combination of horizontal and vertical pulse information intended to control the decoding of a television signal by a display device, recorder or other type of video processing equipment. Usually it is mixed with the video information to produce a composite picture signal (figure 4-2) which is distributed for general use.

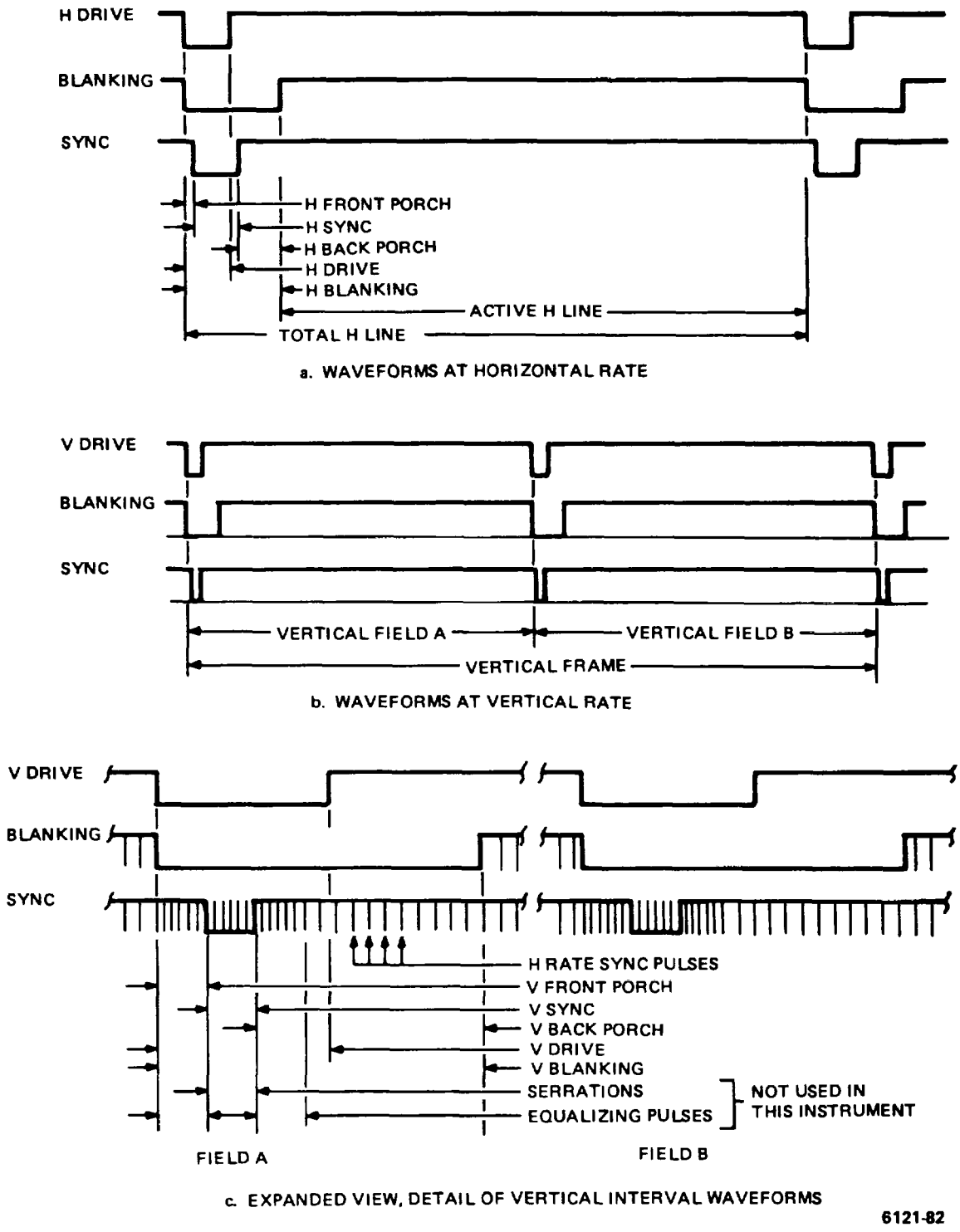
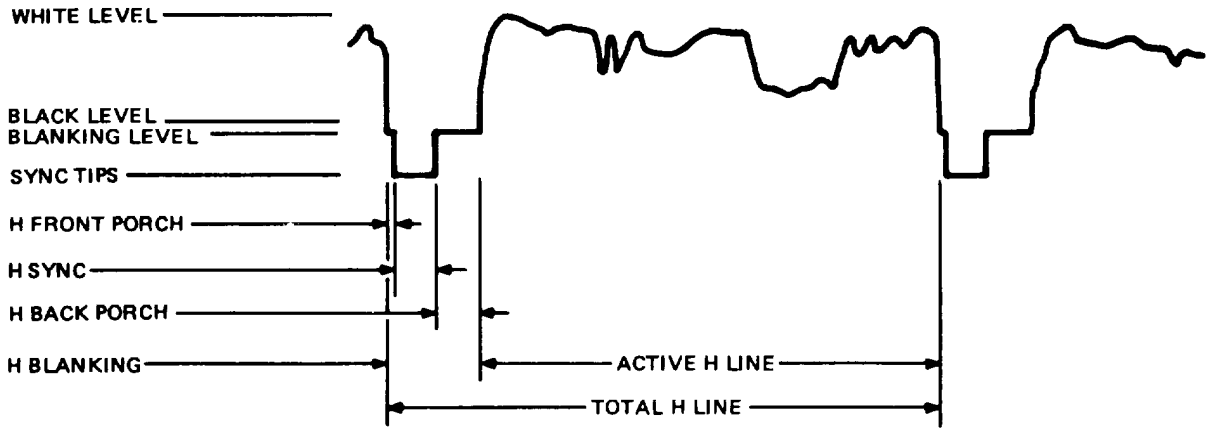
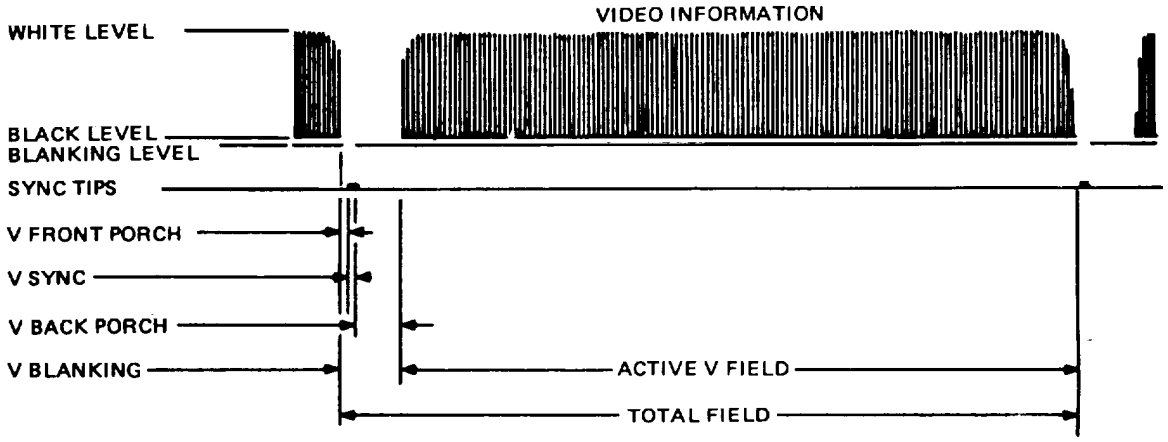


Figure 4-1. Typical Synchronizing Generator Output Waveforms



a. HORIZONTAL SCANNING LINE RATE



NOTE

The basic video signal is composed of video, blanking and sync as shown above to form the "composite video signal". Various significant parameters and common terminology applied to them (such as "front porch' and 'back porch") are outlined above. In some instances, a "non-composite" video signal may be used which is the same as that shown above less the sync portion, composed of only the video plus blanking.

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Figure 4-2. Typical Video Waveforms

The description of a scan rate will specify the number of scanning lines per frame and the vertical field rate. Most television systems are "interlaced" to avoid a visible flicker in the display, usually a 2:1 ratio (figure 4-3). Thus, 2:1 interlace ratio means that two entire display "fields" must be developed to generate one "frame", or complete image. For example, the scan rate of 675/60 indicates that: - There are 675 scanning lines per television frame.

- The field rate is 60 Hz. That is, one television field is developed in 1/60 second.

- Interlace ratio is 2:1. The frame (a complete image) will be composed of two fields. Therefore, one frame is produced in 1/30 second. Each field is composed of half the number of scanning lines per frame, as in this example 337.5.

NOTE

The format for this instrument: H drive, V drive and blanking is the same for all rates. The sync waveform is the INDUSTRIAL format without equalizing pulses and serrations per EIA Standard RS 343A (see figure 4-4).

Horizontal rate pulses are adjustable so the waveform can be matched exactly to the desired operating format. Vertical pulse proportions must by synchronous with the horizontal scan lines, and therefore are determined by digital count and adjustable by count selection.

In order to provide interlace, the master oscillator (on the drive/blanking card) operates at a multiple of twice horizontal (2H) rate. The serrations and equalizing pulses are developed directly from this master timing reference, at the 2H rate. From this point, the master timing pulses are divided by count to generate horizontal (H) rate and vertical (V) rate pulses. Horizontal rate pulses are adjustable to allow operation at various formats as required for different scan rates. Vertical rate pulses are established by scan line count.

The 2H timing reference is used to develop the serration pulse, and also a front porch pulse somewhat shorter than the serration width to act as a timing reference for blanking and drive pulse leading edges.

The 2H front porch pulses are submitted to a 2:1 count to develop H-rate timing reference for generation of blanking; H drive and H sync; these particular pulses are generated by individual monostable multivibrators on their respective circuit cards.

These 2H rate pulses are also applied to a counter which develops the vertical (V) rate. This circuit develops a V reset which acts as the trigger to generate vertical pulses which signify the end of a television field (two fields constitute a frame which is one complete

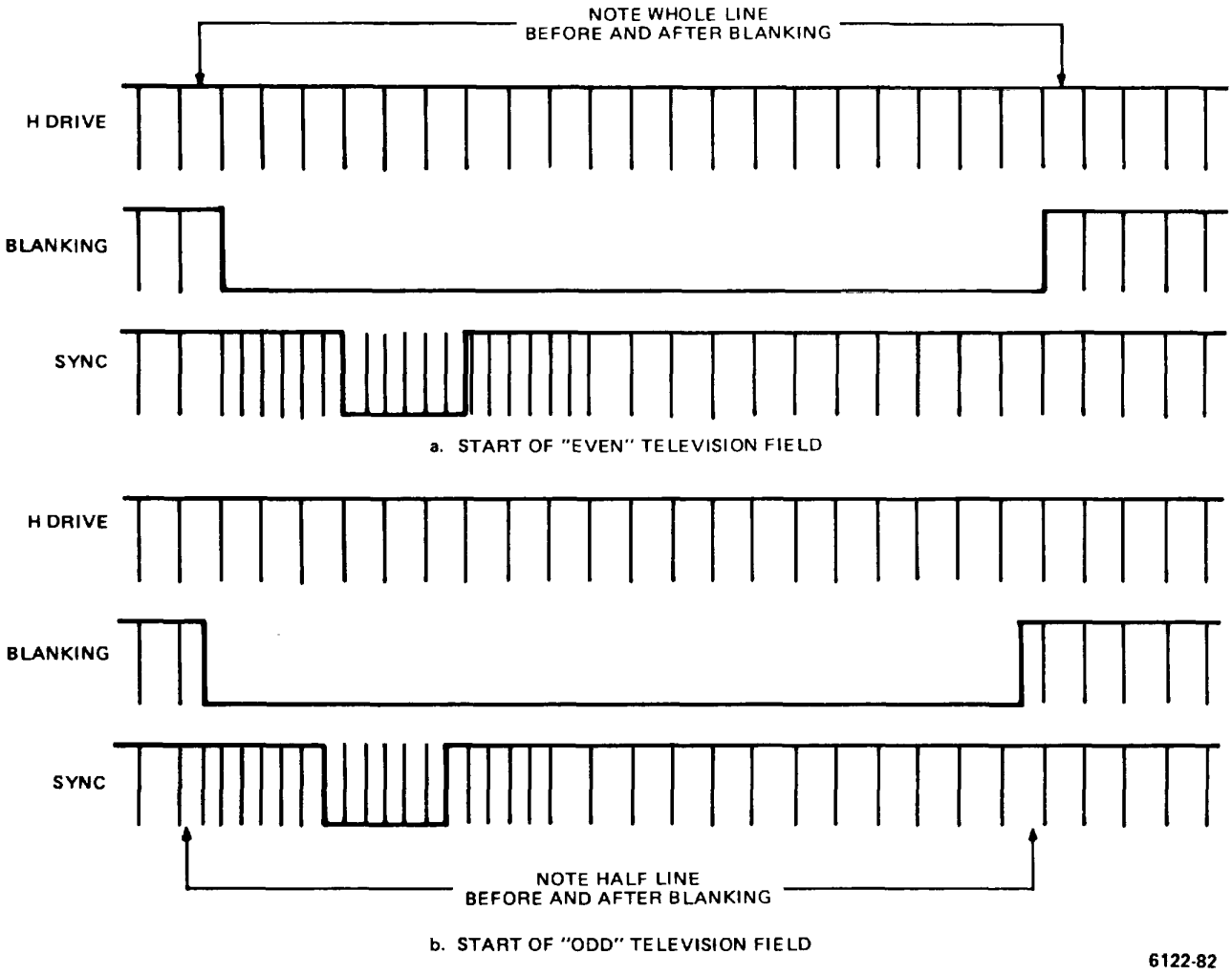


Figure 4-3. Detail of 2:1 Interlace

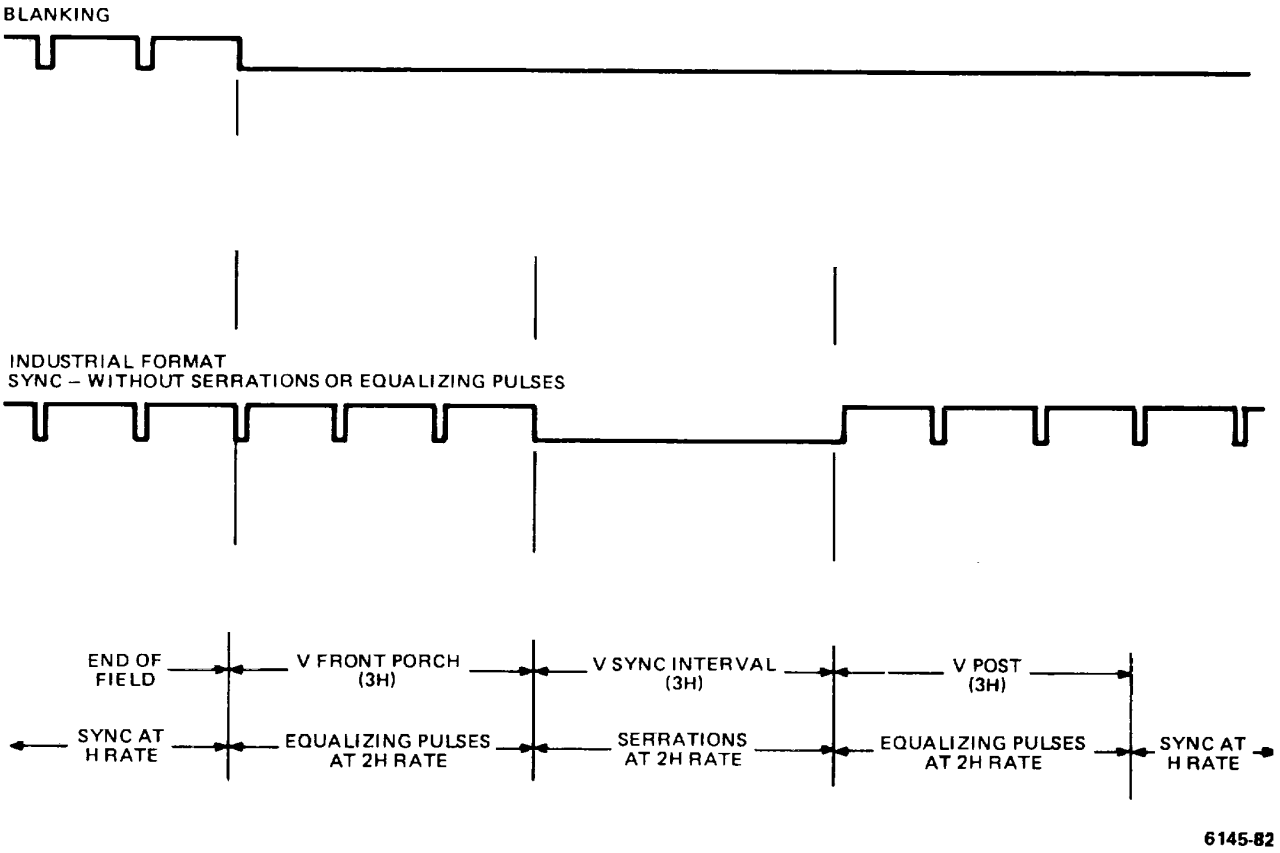


Figure 4-4. Detail of Vertical Sync Interval

presentation in the vertical dimension of the television raster). Interconnections are provided on the sync count card to determine the number of horizontal lines in the frame.

Vertical pulses, initiated by the V trigger, are controlled for proper width by count of horizontal lines. A matrix is included on the sync count card to control width of the V blanking and V drive pulses. The V sync pulse is at all times delayed by a 3H front porch from the start of V blanking and always is 3H (the time of three horizontal lines) in width.

4-3. Pattern Generator. (See figure FO-2). Synchronizing information is received at the pulse input card where the pulses are processed to correct polarity, dc level, and pulse width for generation of the signals as desired. A basic horizontal gate is developed from H drive to control horizontal pattern elements, and a vertical gate is developed from V drive for development of vertical elements. The blanking signal is processed for development of the pedestal (setup) in the composite and non-composite video signal; the level is adjustable on the video card. Blanking also is used for synchronizing of the resolution signals to provide the most stable signal possible. The sync signal is processed only for addition to the output video signal, if a composite video signal is desired at the output. The level of this pulse may be reduced to zero by a control on the video card to develop a non-composite video signal.

The circuits develop the various individual patterns and are contained on separate removable plug-in circuit cards. The basic amplitude control and the gray scale signal, which is analog in nature, is developed by the gray scale control, gray scale and other associated control cards. The complete analog signal is routed to the level control on the control panel to determine the amplitude of the video portion of the output signal. This signal is submitted to the video card where it is mixed with other digitally formed pattern elements to develop the complete video portion of the output signal. If the gray scale waveform is not being used, the gray scale control card produces only a dc level that is used to clip off digital pattern elements, acting as an amplitude (video level) control.

The digitally derived patterns with selectable polarity (bar, dot, H bar, V bar, window, V stripe and H stripe) are routed to the polarity card where either white or black pattern elements are developed as desired, when routed to the video card.

The resolution signals are emitter coupled from the separate resolution cards directly to the video card to preserve the very fast rise and fall times of these signals.

Section II. DETAILED CIRCUIT DESCRIPTION

4-4. Sync Generation. The master oscillator circuitry develops a pulse train from a stable crystal-controlled oscillator circuit whose risetimes act as the timing reference for generation of all waveforms. The crystal-controlled master oscillator is located on the drive/blanking card (figure FO-3), operating at 200 times the horizontal rate. The 200H pulses are counted to 20H by a decade integrated circuit counter, then the 20H pulses are counted down to 2H by counter Z3.

EIA Standard RS-343 requires that serrations of horizontal rate be produced during the sync interval. Serration polarity is opposite that of the horizontal pulses to permit detection of the vertical sync. Therefore, the negative trailing edge of the serration pulses becomes a sync timing reference as opposed to the negative leading edge of the horizontal sync pulses. The 2H pulses from the master oscillator are routed to a monostable multivibrator where a delay is produced to generate the serration pulse width. From this point on, the trailing edge of the serration pulse is used as the sync timing reference. However, the leading edge of blanking must take place previous to the timing reference. Therefore, a second monostable multivibrator develops a time delay to generate the proper start of blanking. This control establishes the width of horizontal front porch (time from start of blanking to start of sync).

The 2H pulses are routed to the serration monostable (Z9) and front porch monostable (Z10) on the sync card (figure FO-4). The front porch pulse trailing edge becomes the timing reference for horizontal and vertical blanking. Integrated circuit counter Z5B on the sync count card (2:1 count) (figure FO-5), develops the H rate timing reference applied to the H drive monostable (Z7) and to the H blanking monostable (Z8) on the drive/blanking card.

Development of an interlaced synchronizing waveform requires that the vertical information be counted from the horizontal. Therefore, the reference timing edge for blanking is routed to the sync count card for this operation.

The sync count card (figure FO-5) contains a series of integrated circuit J-K flip-flops to count the proper number of horizontal lines which will be developed in each vertical field. A different count is required for each scanning rate. This is accomplished by utilizing a group reset technique. Outputs from the counter stages Z5 through Z10 (except Z5B) are applied to a control gate that is connected to a common buss (Z2). A mixture of different counted pulses is then acquired which develops a reset pulse after an appropriate interval, according to programming jumpers that determine which counts are applied to the gate. A matrix is provided on the card for selection of the reset counts as desired for any one scan rate. The reset pulse is developed by monostable Z1 and routed to the J-K flip-flops where all elements in the counter are reset simultaneously. The trigger resulting from this reset is then used for initiation of vertical pulses.

The trigger obtained at the counter reset is routed to the drive/blanking card for initiation of V blanking at bistable multivibrator Z6C and Z6D. It is essential that the long blanking pulse be controlled in synchronism with the horizontal scanning to prevent apparent jitter in the television display. Therefore, a proper selection of pulses is taken from the earlier stages of the sync count card and routed to the control gate Z4 to time the end of the V blanking pulse developed by the bistable on the drive/blanking card. Pulse width is controlled by matrix interconnection on the sync count card.

The V drive pulse is developed by the same technique as V blanking. The trigger pulse developed by monostable Z4 on the drive/blanking card is routed to bistable Z6A and Z6B to start the V drive pulse. Timing pulses selected from the J-K flip-flop counters control gate Z3 on the sync card. The gate output is routed to gate Z6B to turn the bistable off, completing the V drive pulse which is then routed out of the card through isolating stage Q3.

The vertical and horizontal blanking pulses are then combined to gate Z5D on the drive/blanking card to provide a mixed blanking signal. Horizontal and vertical pulses are also routed out of the card as needed to initiate other actions by jumper selection of output stages Q1 through Q7.

A vertical sync pulse is developed within the vertical blanking interval and is delayed 3H from the start of blanking and with a duration of 3H. Multivibrators in the sync card produce the front porch delay and the vertical sync width. It is a further requirement that the vertical sync pulse be absolutely locked to the horizontal scanning rate. Pulses from the sync count card are then used to control bistable multivibrators which develop the vertical sync timing relationships. Bistable Z2A and Z2B produces a pulse three lines long (V front porch), Z1A and Z1B produces a six line pulse, and bistable Z3C and Z3D produces a nine line pulse. Gate Z3A combines the three line and six line pulses to one which extends from the third to sixth line in the vertical interval for the V sync pulse. Gate Z3B combines the nine line pulse with the V sync pulse to make two pulses, one from the start of the vertical interval to the third line, and another from the sixth to ninth lines. This pulse series is used to control the insertion of equalizing pulses before and after V sync.

The equalizing pulses, at 2H rate, are developed by monostable Z5 and triggered by the trailing edge of the front porch pulse developed by multivibrator Z10. The horizontal sync pulse is developed similarly by monostable Z4 at 2H rate and counted down to H rate by gate Z8D.

All of these components, i.e. H sync, 2H equalizing pulses and serrations are combined into the sync waveform in one of three selectable formats:

a. With Equalizing Pulses and Serrations. H sync pulses are transmitted through gate Z7B except from the first to ninth lines of

the vertical interval, as determined by gate Z8B. Equalizing pulses at 2H rate are introduced from the first to third and sixth to ninth lines through gate Z8C which is controlled by inverter Z6D, using the control pulse from gate Z3B. Serrations at 2H rate produced by monostable Z9, are inserted from the third to sixth lines of the vertical interval by gate Z7A.

b. Without Equalizing Pulses and Serrations. Equalizing pulses are not permitted through gate Z8C, which is turned off by inverter Z6C, in turn controlled by grounding the inverter input at resistor R12 (pin M). This also turns off gate Z8B and turns on Z7C, deleting sync pulses from the third to sixth lines of the vertical interval, substituting H-rate sync pulses for the 2H equalizing pulses.

Serrations are blocked from passing through gate Z7A by the control level at R9, as controlled by inverter Z6F and the voltage at R8 (pin T). A vertical sync pulse without H or 2H information results.

c. Military Waveform. The sync waveform used in certain systems requires that there be no H rate of 2H content in the vertical front porch and that there be no equalizing pulses and serrations as well as no horizontal front porch. Pins M, T and U are grounded as in (b). The sync pulse is developed by Z4, triggered by the output of gate Z8A. This gate combines the serration and front porch pulses so that Z4 will be triggered by the longer of the two pulses usually serrations. However, gate ZID blocks the serration pulses, causing Z4 to be triggered by the trailing edge of the front porch pulse, coincident with the start of blanking and drives. Gate Z7D normally would be blocked by low voltage at pin N. When it is not blocked (+5v at pin N), gate Z7D deletes the sync pulses during the vertical front porch as commanded by the output of bistable Z2A and Z2B.

Sync generator outputs (H drive, V drive, blanking and sync) are processed through the pulse output card (figure FO-6) to properly drive coaxial cable at the required amplitude and impedance. Four identical circuits are used. For instance, the H drive pulse input is routed from pin B through bias network R1 and R2 to Q1. The collector waveform from Q1 is routed to push-pull output drivers, Q2 and Q3. Diodes CR1 and CR2 compensate for the base-to-emitter drop of the output drivers. Series resistors R4 and R5 provide the proper cable drive source impedance, and R6 provides a ground return path. The output is ac coupled through C1 to the output (pin W). Pulse amplitude control is obtained by the voltage level applied to collector load R3 established by series regulator Q13, and controlled by potentiometer R25.

4-5. Basic Video Signal Development. The incoming H drive, V drive, blanking and sync signals are routed to the pulse input card (figure FO-7) where the pulses are processed to uniform level and risetime. The outputs from this card are separated into vertical and horizontal components which control all subsequent operations in signal development. The card contains four identical circuit sections.

Each input signal is applied to an isolating emitter follower which biases the pulse signal so that pulse tips are negative (below ground level). The emitter-follower outputs then control modified bistable multivibrators in which the negative pulse tips lock the multivibrator into a predictable mode. A modified Schmitt trigger operation is achieved with a uniform level output of sharp risetime. The outputs are then routed to appropriate pattern generation circuitry. For instance, the sync signal is applied to emitter-follower Q1 where impedance is transformed and biased. The pulse is then routed through diode CR1 to the base of Q2 where the negative tip locks operation of the bistable in one direction with Q2 collector "high". Transistor Q3 is saturated to the "low" state by current through R8. When the negative pulse ends the emitter of Q1 goes high and Q2 is biased "on" through R5. Since voltage at the base of Q2 is limited to the base-to-emitter drop, Q1 becomes reverse biased. Transistor Q3 then becomes non-conductive with the collector going "high". Additional current through R6 reinforces this stable state. The circuit remains in this mode until another negative input pulse tip causes CR1 to conduct again. This circuit operation develops both positive and negative pulses of sharp risetime and uniform amplitude for each of the four input signals.

The video card (figure FO-8) processes all pattern information into the output video signal. Pattern signals are coupled into the card through one of three routes. Most are emitter coupled at the common junction of Q10 and R24 through connector pin W. Emitter coupling allows the fastest risetime, since it is a very low impedance. This is especially important for the resolution function.

The emitter-coupled inputs (pin W) are connected to the output of this stage at the junction of R24 and Q10 emitter, where all video elements are brought to a common point, but inverted. This low impedance point drives Q9, which establishes the proper signal polarity at fast risetimes. The signal is then routed to emitter-follower Q8 and black level clipper R19 and Q7. The clipper is used to adjust digital signal black level as close as possible to the black level of the gray scale signal.

The digital signal is applied to emitter-follower Q2 and the incoming gray scale signal is applied to Q1. The emitter-follower pair operates as a level control, clipping off the digital video signal as directed by the gray scale input from the front panel level control. In this way the video level is controlled without sacrifice in digital signal rise and fall time. The video signal is routed to an emitter-follower network which mixes the blanking and sync signals to form the composite video.

The blanking and sync signals enter the card through pins A and F, and processed in similar fashion. For instance, the blanking signal is routed through bias network R48 and R49 to Q19, whose collector load is connected to -5v, creating a pulse from zero to -5v. If blanking is not used (as in the video only signal mode), Q20 is turned on by switching a -5v level to pin E, creating an "off" level near

ground potential. The signal from common collectors Q19 and Q20 is routed to range limiting resistor R47 and blanking level control R46. The signal is then fed to emitter-follower Q18 which drives the current mixing network through R34. The sync signal is processed by Q3 and Q4 with the level controlled by R11 and fed into the network by R8 to Q6. All three components of the composite signal are formed at R35. Circuit dc levels have been chosen to generate the blanking level (blacker-than-black) at near ground potential.

The signal is routed to emitter-follower Q14, which filters the signal slightly to remove spikes from the very fast rise and fall times (C5) and bias the signal negative to compensate for dc shifts encountered in the output driver. The push-pull complimentary pair driver (Q16 and Q17) is fed by emitter-follower Q15, which also includes diodes CR1 and CR2 to compensate for base-to-emitter voltage drops in the driver transistors. Source impedance is determined by the built-out resistor network R42, R44 and R61.

4-6. Video Processing. Many functions are to be developed in either a white or black pattern format (bar, dot, window, H stripe, V stripe, etc.). The circuitry on the polarity card (figure FO-9) performs this function as well as developing the flat field function. Digital signals from various function circuits are developed at R29 (pin Y). They are fed to emitter-follower Q10 which is biased negatively through R27 and R28. When white level is developed, the emitter of Q10 is high, thus back-biasing diode CR7. When Black level is developed the emitter of Q10 goes low, allowing CR7 to conduct. Transistor Q3 is then turned "off", causing a high level to be developed at the collector of Q3, and a low level at the collector of Q2. Therefore, both polarities of signal are available; inverted at Q3 and non-inverted at Q2. Selection is made through stages Q1 and Q4 which have a common collector load (R15). If voltage is applied to R10 through pin C, the signal is passed through CR2, and Q4 is turned on causing a non-inverted (white) signal to be developed at R15, with Q1 biased off. If voltage is applied to pin L, diode CR1 and Q1 are operational, causing an inverted (black) signal to be developed at R15; Q4 is biased off.

In some cases the digital signal at R15 is locked at white level (as for the flat field and gray scale functions). This is insured by control stages Q8 and Q9. voltage is applied at input pin J through isolating diode CR5 and causes Q8 to saturate, forcing voltage at R1 and R10 low, and therefore, locking both Q1 and Q4 "off". Therefore, the signal at R15 will remain at a high (white) level. Signal information which does not need polarity processing can be inserted at pin P to load resistor R15, such as the reference signal in the resolution function. The signal at R15 is blanked by stage Q5 to ensure video black level through the horizontal and vertical retrace intervals. The signal is inverted by Q6 and fed to emitter-follower Q7 and is routed to the video emitter coupled input.

4-7. Gray Scale. The gray scale function involves the following circuit cards:

a. Gray Scale Control. Clock signal development and analog gray scale output signal processing (figure FO-10).

b. Gray Scale. Ring counter to clock off location of each gray scale step (figure FO-11).

The gray scale signal is developed by the gray scale control and gray scale cards. The -H Gate input synchronizing signal is applied to gray scale control card (pin F) through an isolating diode (CR1) to emitter-follower control stage Q1, which phase locks an astable multivibrator to develop the rate at which bars will be developed. During the active television line a high level is present at the emitter of Q1 and diode CR2 is back-biased and non-conductive. Astable multivibrator Q2 and Q5 operates at a rate established by C1 and C2 and the bias on current control transistors Q4 and Q7. When the synchronizing pulse occurs, the emitter of Q1 goes negative causing CR2 to conduct. This pulls the base voltage of Q2 negative clamping operation of the astable in a predictable state throughout the duration of the synchronizing pulse. When the sync pulse ends, diode CR2 again becomes non-conductive, the base voltage at Q2 charges linearily through R5, Q7 and C1, until Q2 conducts, starting normal astable operation. The time interval of this constant current-charging multivibrator is controlled by divider R1 and R2. Pulses developed by this astable multivibrator are used to control an integrated circuit ring counter on the gray scale card which controls formation of the gray scale waveform.

The gray scale waveforms developed at R17 on the gray scale control card by the gray scale card is applied to an isolation emitter-follower Q10 and a black level clipper Q11, which sets the black level at ground. The companion transistor pair Q8 and Q9 sets the maximum white level as controlled by R23. The resultant signal is output from the card through driver Q12 to the level control potentiometer on the front panel and subsequently to the video card.

The clock signals are routed to the gray scale card through pin N to gate Z6A, where it is processed to drive the clock inputs of J-K flip-flops which make up a ring counter (Z1 thorugh Z5). The ring counter produces pulse sequentially with the output "stepping over" one element for each cycle of the clock input. Integrated circuit J-K flip-flop Z3B is used to develop pulses to start ring counter operation. Section Z3A develops the first pulse after blanking which normally is a black level step at the start of the gray scale.

Gray scale steps are formed by saturating stage Q1 through Q8. The output pulse of Z1B at pin 9 is positive, causing Q1 to turn on. The gray level is determined by the control (R1) setting. At the next clock cycle, transistor Q1 will turn off, and Q2 will be turned on by the ouput of Z1A due to ring counter cycling. Then the gray scale level will be determined by the setting of R2. This sequence continues through controls R3 through R8. The gray scale characteristic is set by each control adjustment.

The ring counter will have completed a cycle within one active tv line time, but not absolutely. Therefore provision is included to reset the ring counter to the initial state at the end of each line. A positive H gate signal is routed to pin P to inverter Z6B, where it is inverted and routed to clear all ring counter elements.

Usually it is desirable to generate black level during the horizontal and vertical blanking intervals and at the start of each line continuously until the second step occurs; bistable multivibrator Z6C and Z6D is used for this purpose. The reset pulse from Z6B sets the bistable to produce a positive dc level at Z6 (pin 8), causing stage Q10 to turn on and thereby develop a black level digital signal. The bistable is forced to the other state by the output from ring counter step Z1B, routed from card pin T to pin E. Black level is set in the analog gray scale channel by turning on Q9. Depending upon the application, this can be through the blanking interval by connecting jumper 1-2 (the normal conditon) or only for duration of the ring counter step 1 by connecting jumper 2-3.

4-8. H Bar, V Bar, Bar and Dot. These functions are developed by the H bar (figure FO-12) and V bar (figure FO-13) cards. The particular patterns are selected by logic circuits and pattern proportion is controlled by front panel controls. Horizontal elements in the pattern are developed by the H bar card. This card contains an adjustable monostable multivibrator Q5 and Q8 which determines the width between lines in the vertical dimension of the raster. At the end of the monostable period, a gating condition exists at control transistors Q9 and Q10 which permits triggering of bistable multivibrator Q11 and Q12 to the "on" state for one horizontal line period. The bistable is switched "on" at the start of an active scanning line by h-rate triggers developed by Q15. Triggers developed through capacitor C7 and diode CR7 insure that the bistable is returned in the "off" state at the end of each tv scanning line activated. At the end of this line the monostable operation is again initiated through C2, prohibiting pattern generation for the duration of the monostable period. The monostable active period is determined by the time required to charge capacitor C4 to a voltage level which allows Q5 to conduct. The C4 rate of charge is determined by constant current network R26, and Q6 with current flow established by voltage at the base of Q6 by divider R14 and R12. During the vertical blanking interval the monostable circuit is clamped to a variable dc control level by a clamp circuit which employs the field effect transistor Q3 operating in the enhancement mode. The controllable clamp level is established by Q4 and CR2 from the input voltage at pin D and then connected to the base of Q5 through emitter-follower Q16 which determines position (phase) of the pattern on the raster. Transistors Q1 and Q2 develop the clamp control pulse to control field effect Q3. This pulse swings from +5v to -5v, developing nearly zero impedance across Q3 when the pulse is at the +5v level. Therefore, operation is locked positively to the vertical and horizontal pattern elements.

The V bar card controls development of vertical elements in the test patterns. This card contains a voltage controlled astable multivibrator Q1 and Q4 which runs freely during the active line time. The repetition rate is established by current control transistor Q3. During the horizontal and vertical blanking intervals, the astable multivibrator is clamped to a control voltage which establishes the position (phase) of the pattern in the horizontal dimension of the raster. The clamp circuit incorporates a field effect transistor (Q5) operating in the enhancement mode to connect the control level to the base of Q4 during the blanking interval. The control level determines the time required for Q4 to initiate cycling after blanking, effectively positioning the pattern on the tv line. The level is introduced through pin U to emitter-follower Q16, which includes zener diode CR8 to produce a drop in the 0 to 5v input voltage. Thus the voltage at R40 remains negative throughout the range of control.

Proper operation of the clamp transistor Q5 requires a control pulse which swings from +5v to -5v. The clamp pulse at pin T is then routed to saturating stage Q15. The signal at the collector of Q15 is biased by R5 and R6 to turn on Q14. This pulse, swinging from near 0 to -5v is used to control Q13 whose emitter is referenced to -5v. The pulse at the collector of Q13 swings from +5v to -5v, and is used to control Q5.

Each cycle of the astable develops a trigger from monostable multivibrator Q7 and Q8 which develops the precise sharp pulse required to produce a fine line or dot at all scanning rates. Monostable outputs and H bar pattern elements from the H bar card are combined on the V bar card logic circuits to form the pattern selected. If V bars are to be formed, the monostable Q7 and Q8 operates for each tv line. No voltage is applied to pin L of the V bar card or to pin W of the H bar card, so H bar elements do no appear. To produce the bar pattern, voltage is applied to pin L of the V bar card. Monostable Q7 and Q8 operates as V bars, but H bars are applied through CR7 to Q11, which turns on and locks the monostable to produce the H bar element.

To produce dots, the monostable Q7 and Q8 is allowed to operate only on selected lines. The H bar element is developed at Q3, as voltage is applied to pin W on the digital H bar card. This pulse is routed through bias resistors R26 and R27 to Q10, which clamps the monostable in the opposite phase and prohibiting pattern output. When dots are to be produced, the clamp is released for those horizontal lines.

To produce H bars only, both clamp transistors are used, locking the monostable in one phase and then the other, preventing development of any V bar elements.

4-9. Resolution and Multiburst. Development of the various resolution patterns involves the interrelated action of the resolution (figure FO-14), multiburst (figure FO-15) and multiburst clock (FO-16) cards.

Basically the resolution pattern is the alternate black and white video developed by the output of an astable multivibrator. One resolution card is produced for each burst rate with selected components to produce the desired repetition rate. Additional control circuitry is included on these cards to control generation of the exact signal format desired. The multiburst and multiburst clock cards develop the control functions which are distributed to these control components, and the multiburst card performs other auxiliary functions, including development of the video level produced between bursts.

The multiburst card contains a clock multivibrator Q2 and Q7 which is synchronized to the horizontal blanking by clamp circuit Q1 and CR1. Pulses from this controlled astable control the width of resolution signal bursts and the space between bursts. Repetition rate is adjustable by divider R1 and R11 which controls constant current transistors Q4 and Q5 to permit multiburst development within the active scan line time for the particular scan rate in use. This duty cycle is directed for the various resolution cards by emitter-follower Q12 after processing through Q8, Q9 and Q11 to insert blanking. If separated resolution bursts are to be developed, the astable operates in normal fashion, being clamped to the input H-rate control at CR2 during the H blanking interval. For generation of a continuous pattern, voltage is removed from the clock processing Q8. Therefore, only the blanking waveform is developed at the collector of Q10.

The reference function is a black/white pulse output at the clock rate. Selection of the reference function applies voltage to collector load resistor R33 through isolating diode CR4, causing a signal to be developed at output stage Q13.

All resolution cards are identical except for component values (C5, C3, R3, R4, R10 and R22) which are selected to provide the desired repetition rate. Signals are developed by astable multivibrator Q13 and Q21 and are routed to isolation emitter-follower Q22 to the signal buss. Resolution signals are routed to the emitter-coupled input of the video card. The astable is controlled by clamp diode CR3 and emitter-follower 010. Whenever Q10 develops a signal below ground level, CR3 conducts and the base of Q13 is locked in the "off" state, forcing the astable to remain inoperative. When Q10 develops a higher level of voltage, CR3 is non-conducting, effectively isolating the control stage and permitting the astable to operate normally.

Control signal for the astable Q13 and Q21 is processed by Q11 and Q12. The duty cycle of signal development is established by the signal from the multiburst circuits as directed through R32 to Q12. In turn, load resistor R26 controls the output level of emitter-follower Q10 through bias network R27 and R29. When Q12 turns on due to a "high" condition of the input duty cycle signal, a low level is developed at the emitter of Q10, clamping the astable. When Q12 is biased "off", the astable is operative.

Development of the multiburst signal requires that each resolution card operate in proper sequence. An integrated circuit ring counter on the multiburst clock card is used for control to develop the multiburst signal sequence. Additional control is provided to load resistor R26 through Q11. Transistor Q11 clamps the astable inoperative. At the proper time, Q11 is turned "off" and control stage Q10 then permits the astable to develop a burst.

The basic clock signals for the multiburst ring counter is developed on the multiburst card. Clock and reset signals are developed by Z1C and Z1D. The ring counter is reset at the end of every tv line to assure a proper start for each horizontal line regardless of the circuit condition at the end of the previous line. Flip-flop Z2B develops an initial prime pulse to command the first stage of the ring counter Z2 to operate. The X3B stage controls development of the white-black reference bar at the start of the multiburst array.

The multiburst clock card contains logic to terminate the sequential multiburst operation after the occurrence of the last burst sequence. Integrated circuit Z8A (J-K flip-flop) is the last stage of the ring counter which controls resolution card operation. When this stage operates, flip-flops Z9A and Z9B change state, causing Q14 on the multiburst card to turn on, developing a low state at the emitter of Q1 and stopping clock operations at the end of the multiburst sequence. The ring counter reset (occurring during the blanking interval) returns Z9A to the "off" state. Transistor Q15 provides normal blanking control to the multiburst card.

The multiburst card also contains auxiliary circuits to operate the resolution cards. Transistor Q12 generates the level of gray which will be presented between bursts. Transistor Q18 develops a black level between bursts when minimum APL is selected. These are controlled by transistors Q20, Q21, Q22 and Q23 as dictated by inputs from the clock to properly phase the video (Q22), the ring counter (Q20) to prohibit development of a gray level after the multiburst is complete, (Q23) to prohibit operation during the continuous mode.

Provision is made to switch a reference segment into the multiburst mode. Voltage is applied to counters Z1, Z2 and Z3 of the multiburst clock card to locate the reference segment. The positive pulse is routed to Q11 on the multiburst card to inhibit resolution pattern development. The negative pulse is routed to Q17 to permit development of the reference information by Q13 at the proper time; voltage is applied to R33 also.

4-10. H Stripe, V Stripe, and Window. The window pattern is developed with reference to the top and the left edge of the television raster. Basically, generation is accomplished by two H and two V monostable multivibrators. The first one times the spacing from the top (or left edge) of the point at which pattern is developed, and the second establishes the time through which the pattern will be generated. The appropriate circuits, including mixers, are placed on the H window (figure FO-17) and V window (figure FO-18) cards.

The V stripe pattern is the horizontal component of the window pattern presented for the entire vertical dimension of the raster. This pattern is obtained by operating the H window card with the V window card not energized.

The H stripe pattern is the vertical component of the window pattern presented for the complete horizontal scan line. In this case the V window card is operated without the H window card energized.

The window pattern is developed when both the H window and V window cards are energized. Outputs are routed through Q12 (pin L on both cards) to common load resistor R29 on the polarity card (figure FO-9). The mixture of H stripe and V stripe components results in the window pattern, a square at the center of the display raster.

H window and V window cards feature monostable multivibrators with a constant current charging network to provide a wide control range. A control network is provided on each of these cards for adjustment of position and size; bias resistors R16 and R17, current control transistor Q5, and current limiting resistor R15 on the H window card are components typical of control range circuitry.

In the H window card a trigger spike is developed from the negative input horizontal gate through isolation diode CR1, inverter Q1 and differentiator C1. The spikes are applied to a bias network and subsequently through the input horizontal gate through differentiating capacitor C1. The spikes are applied to a bias network and subsequently through diode CR3 to the monostable multivibrator Q4 and Q7, which determines the time from the left edge of the raster to start of the window. The end of this cycle develops a trigger through isolation stage Q3 to start monostable Q8 and Q11 which develops the horizontal window segment. The output is routed through control circuitry CR5 and R36 to output stage Q12.

The position of the window in the vertical plane (from the top of the raster) is developed by multivibrator Q1 and Q4 on the V window card, whose cycle rate is determined by constant current control transistor Q2 and divider R4 and R5. The window spacing (width) is developed similarly by monostable Q8 and Q11 as controlled by R30 and R36. The pulses must be locked to the horizontal line rate to prevent a drift or visible "run through" of pattern as displayed. Horizontal rate triggers are routed through diode CR4 and blanked by CR3 until the monostable position cycle is complete. The bistable Q6 and Q7 was started by the -V gate signal, and is returned to original state by triggers submitted through C4 and CR6. The transition of -V position signal at the collector of Q7 is routed through CR9, C8 and CR8 to start monostable Q8 and Q11, whose cycle time duration is set by C7, Q9 and divider R30 and R36. Bistable Q13 and Q14 is allowed to operate during this time, as CR15 does not blank out horizontal rate triggers passed through CR14. The bistable Q13 and Q14 starts at the start of each line (triggered through CR11) and stops at the end of the line (triggered through CR12).

4-11. Power Regulation. (See figure FO-19). The power supply employs three separate voltage regulator circuits: +12vdc, +5vdc and -5vdc. The regulators are mounted on a heat sink filter assembly located on the inside rear panel of the cabinet. The +5v and -5v supplies operate from the same transformer (T1) windings with diodes (CR1-CR4) polarity providing positive and negative dc voltages as desired. A separate winding is provided for the +12v supply regulator (Z1) .

Diodes CR1 and CR2 and filter capacitor C8 (located on the heat sink filter assembly) develops a dc level of about +17v reduced by positive regulator Z1 on the rear panel to +12v. This rectifier is kept lightly loaded to keep ripple valleys well above possible regulator dropout levels.

Diodes CR3 and CR4 and filter C7 on the rear panel heat sink develop a negative voltage of about -17v which is reduced by negative regulator Z3 to -5v.

The regulated +12v is used as a reference to operate a precise low ripple (1 mv or less) +5v to operate voltage controlled astable multivibrators which develop the test pattern circuit elements. The +12v dc level is routed through dropping resistor R4 (pin Y) on the power regulator circuit card to zener diode CR5. This reference level is then routed through an adjustable voltage divider (R1) to one side of transistor pair circuit Q2 and Q3. The adjustable voltage at the base of Q3 develops a reference level through the emitter of Q3 to resistor R5. The +5v level is fed back into the base of Q2 to establish a base-to-emitter bias level for controlling the current through load resistor R6. This, in turn, controls the collector voltage for amplifier Q2, which feeds a controlling level to the base of Q1 to the base of power regulator transistor (Q1) mounted on heat sink assembly. From the emitter of the power transistor (Q1), voltage is distributed throughout the unit, and is returned to the power regulator card as a very precise +5v reference level which exhibits less than 1 millivolt ripple.

CHAPTER 5

ORGANIZATIONAL MAINTENANCE INSTRUCTIONS

5-1. Introduction. This chapter contains the organizational maintenance instructions for the test pattern generator. They include routine checks, preventive maintenance checks, and services and general cleaning instructions.

Organizational maintenance of the test pattern generator is limited to fuse replacement. Other maintenance procedures must be performed by general support maintenance in Chapter 6.

5-2. Tools and Equipment. The tools and test equipment allocated for maintenance on the test pattern generator are listed in the Maintenance Allocation Chart in Appendix B. There are no special tools or test equipment required for maintenance of the test pattern generator.

5-3. Preventive Maintenance Procedures.

a. General. Operator and organizational preventive maintenance is the systematic care, servicing, and inspection of equipment to prevent the occurrence of trouble, to reduce downtime, and to maintain the equipment in serviceable condition.

b. Routine Checks. Routine checks such as: cleaning, dusting, washing, checking for frayed cables, stowing items not in use, covering unused receptacles and checking for loose nuts and bolts are not listed as preventive maintenance checks or services. These are things that you should do anytime you see they must be done.

c. Preventive Maintenance Checks and Services. Preventive maintenance checks of the test pattern generator are not required.

5-4. Cleaning.

WARNING

USE OF CLEANING SOLVENT

Fumes of TRICHLOROTRIFLUOROETHANE are poisonous. Provide adequate ventilation whenever you use TRICHLOROTRIFLUOROETHANE. Do not use solvent near heat or open flame. TRICHLOROTRIFLUOROETHANE will not burn, but heat changes the gas into poisonous, irritating fumes. DO NOT breathe the fumes or vapors. TRICHLOROTRIFLUOROETHANE dissolves natural skin oils. DO NOT get the solvent on your skin. Use gloves, sleeves and an apron which the solvent cannot penetrate. If the solvent is taken internally, see a doctor immediately.

a. General Cleaning. Use a dry, clean, lint-free cloth or brush to remove dust or dirt. If necessary, moisten the cloth or brush with trichlorotrifluoroethane (FSN 6850-00-105-3084). After cleaning, wipe dry with a clean cloth.

WARNING

Compressed air is dangerous and can cause serious bodily harm. It can also cause mechanical damage to the equipment. Do not use compressed air to dry parts where trichlorotrifluoroethane has been used.

b. Compressed Air. Dry, compressed air, not to exceed 29 psi, may be used, unless otherwise indicated, to remove dirt and dust from inaccessible places.

5-5. Touch-up Painting. Remove rust and corrosion from metal surfaces by lightly sanding them with fine sandpaper. Brush two thin coats of paint on bare metal to protect it from further corrosion. Refer to the applicable cleaning and refinishing practices specified in TB 746-10.

5-6. Removal and Replacement. Organizational repair is limited to fuse replacement. Perform the following procedure to remove and replace indicator lamp.

a. Fuse Removal. Perform the following procedure to remove fuse:

(1) Slide the clear plastic fuse cover (located at the rear of the unit) to the left (see figure 2-2).

(2) Pull the fuse release lever to the left and remove the fuse. The fuse is a 2A SLO BLO 3AG.

b. Fuse Replacement. Perform the following procedure to replace fuse:

(1) Pull the fuse release lever to the right.

(2) Insert fuse in fuse holder.

(3) Slide plastic fuse cover to the right.

(4) If the fuse continues to blow or the unit does not function, refer to Chapter 6 for general support maintenance.

CHAPTER 6

GENERAL SUPPORT MAINTENANCE INSTRUCTIONS

Section I. GENERAL

6-1. Introduction. Maintenance of the test pattern generator is performed at three levels: Organizational, General Support and Depot. This chapter provides instructions for general support maintenance only. General support maintenance is performed by those maintenance activities designed to support the using organization and emphasizes corrective maintenance at the equipment site. General support maintenance personnel perform corrective maintenance on items which are identified as faulty by organizational maintenance personnel, but are beyond their capability to correct using the maintenance resources authorized at the organizational maintenance level. General support maintenance personnel also provide technical assistance to the using organization in all areas which require skills and training that are beyond the capabilities of the organizational maintenance personnel. General support maintenance is limited to the activities described below:

a. Replace an unserviceable subassembly, module, assembly or unit with a like subassembly, module, assembly or unit.

b. Perform the repairs and adjustments required to correct a specific failure or unserviceable condition and restore an item to a serviceable condition. This function includes soldering or component replacement.

6-2. Voltage and Resistance Measurements. Voltage, resistance, and continuity measurements are made by general support maintenance personnel for troubleshooting faults which cannot be resolved or repaired by organizational level personnel. Normally, such faults are traceable to wiring or chassis-mounted components.

Section II. TOOLS AND EQUIPMENT

6-3. Tools and Test Equipment. Tools and test equipment required to perform the maintenance procedures given in this chapter are listed in the Maintenance Allocation Chart in Appendix B.

6-4. Repair Parts. Repair parts authorized for use by general support maintenance personnel for the test pattern generator are listed in the Repair Parts and Special Tools List (RPSTL), TM 11-6625-3025-24P.

Section III. TROUBLESHOOTING

6-5. General. This section provides the fault isolation and detailed troubleshooting procedures required to identify and correct a malfunction in the test pattern generator. Fault isolation at this level consists primarily of signal tracing, voltage and waveform measurements (refer to Section V). Schematic diagrams for the printed

circuit board assemblies are shown in figures FO-3 through FO-19. Complete wiring interconnection diagrams are presented in tables 6-5 through 6-21 (Section VI).

6-6. Troubleshooting Procedures. Table 6-1 is a list of trouble symptoms that may be encountered due to malfunctions of the test pattern generator. Check the adjustment procedure in Section V to establish that a particular failure has definitely occurred. Often a symptom of difficulty can be traced to improper adjustment.

WARNING

Even low voltages commonly present in transistorized circuits are potentially dangerous. Additionally, full line voltage is present on fuse terminals, power switch terminals and other exposed points within the interior of the unit, and are accessible when the cover of the equipment is removed. Refer to (FO-20 and FO-22) to learn the areas containing high voltage in the equipment. Be careful not to contact high voltage connections when troubleshooting this equipment.

SECTION IV. REPAIR

6-7. Introduction. This section describes the repair instructions for the test pattern generator and consists of removal and replacement procedures for the printed circuit cards, front panel, rear panel and power supply components. Visual aids for the procedures are provided with schematics, parts location diagrams and interconnection wiring lists.

6-8. Removal and Replacement Procedures. See figures FO-20 through FO-23 for component locations and refer to table 6-2 for the wiring interconnection lists during the following removal and replacement procedures.

6-9. Printed Circuit Cards. The printed circuit cards are located in the card file behind the front panel shown in figure FO-20. The cards are positioned in the unit from right to left as shown in figure FO-21. For convenience, table 6-2 references the part number of the card, card location and functional name of each card. The circuit cards may be removed and replaced by performing the following procedure:

a. Removal.

(1) Remove the eight screws securing the top panel to cabinet to gain access to the circuit card file.

(2) Remove the circuit card by grasping the top corners of the card and gently wiggle the card to release from connector. Pull card straight out.

Table 6-1. Troubleshooting

	Trouble	Probable Cause	Remedy
1.	Indicator lamp not illuminated. Power switch in ON position.	a. Fuse b. Indicator lamp	Replace fuse Replace indicator lamp
2.	Indicator lamp illuminated. All sync genera tor waveforms missing (H drive, V drive , blanking and sync	+5V, -5V and 12V power supply defective	Check +5V, -5V and +12V power supply levels
3.	No H drive, V drive, blanking or sync waveforms	a. Master oscillator b. Pulse output circuit card	Replace drive/blanking circuit card Replace pulse output circuit card
4.	Pulse timing and format correct. Amplitude incorrect.	Pulse output circuit card	Adjust pulse output (see figure 6-6)
5.	H drive correct, but V drive, blanking and sync incorrect at vertical rate	Sync count circuit card	Replace sync count circuit card
6.	H drive and/or horizontal rate blanking pulse missing or occurs at 2 H rate	2:1 count circuit card	Replace sync count
7.	H drive or horizontal rate blanking pulses have incorrect width or are erratic	Drive/blanking circuit card	Replace drive/blanking circuit card
8.	V drive or vertical rate blanking pulses incorrect, but H drive and sync waveforms are normal.	a. Sync count circuit card b. Drive/blanking circuit card	Replace sync count circuit card Replace drive/blanking circuit card

Table 6-1. Troubleshooting (Continued)

	Trouble	Probable Cause	Remedy
9.	Blanking waveform is abnormal, but amplitude correct	Drive/blanking circuit card	Replace drive/blanking circuit card
10.	Sync waveform incorrect in format and timing, but amplitude is correct	Sync circuit card	Replace sync circuit card
11.	Video level control voltage low	Gray scale control circuit card	Replace gray scale control circuit card
12.	White and black patterns for: window, bar, dot, V bar, H bar, H stripe and V stripe are abnormal	Polarity circuit card	Replace polarity circuit card
13.	Bar, dot, H bar or V bar function abnormal	a. H bar circuit card b. V bar circuit card	Replace H bar circuit card Replace V bar circuit card
14.	Resolution function abnormal	a. Multiburst circuit card b. Resolution circuit card (10) c. Multiburst clock circuit card	Replace multiburst circuit card Replace resolution circuit card (10) Replace multiburst clock circuit card

NOTE

The resolution cards are emitter-coupled to the video card. A problem on a resolution card may force video to black level resulting in an apparent loss of video while sync and blanking remain at the output. Check for this possibility by removing all ten resolution cards. Other generator functions should operate normally. If the problem was verified, select the multiburst function, then install the resolution cards, one at a time, until the problem occurs. The last resolution card installed is the source of the problem.

Table 6-1. Troubleshooting (Continued)

Trouble	Probable Cause	Remedy
15. Window, H stripe or V stripe function abnormal	a. H window circuit card b. V window circuit card	Replace H window circuit card Replace V window circuit card
16. Gray scale, function abnormal	Gray scale circuit card	Replace gray scale circuit card
17. Difficulty in pattern synchronizing lack of all patterns	Pulse input circuit card	Replace pulse input circuit card
18. Sync or blanking signal abnormal	a. Pulse input circuit card b. Video circuit card	Replace pulse input circuit card Replace video circuit card
19. Improper pattern generation, amplitude, phase ripple or hum, inaccurate sync timing	Misadjustment of power regulator circuit card	Adjust or replace power regulator circuit card (see Figure 6-3)

Table 6-2. Circuit Card Identifier/Function Cross-Reference

Position	Card Number		Function
		Section B	
1	L-2020		V bar
2	L-2004		H bar
3	L-2013		H window
4	L-2014		V window
5	L-2029		Gray scale control
6	L-2028		Gray scale
7		not used	
8		not used	
9		not used	
10		not used	
11	L-2003		Pulse output
12	L-2024		Sync
13	L-2117		Drive/blanking
14	L-2025		Sync count
		Section C	
1	L-2110		Power regulator
2	L-2009		Pulse input
3	L-2012		Polarity
4		not used	
5	L-2011		Video
6		not used	
7		not used	
8	L-2008		Resolution - 10
9	L-2008		Resolution - 9
10	L-2008		Resolution - 8
11	L-2008		Resolution - 7
12	L-2008		Resolution - 6
13	L-2008		Resolution - 5
14	L-2008		Resolution - 4
15	L-2008		Resolution - 3
16	L-2008		Resolution - 2
17	L-2008		Resolution - 1
18	L-2016		Multiburst clock
19	L-2015		Multiburst
20		not used	
21		not used	
22		not used	

b. Replacement.

WARNING

Circuit cards are keyed and cannot be inserted backward. An attempt to force the card in the wrong way will result in a broken connector.

(1) insert card into the proper slot and slide the card in until it mates with connector.

NOTE

Ensure card is seated firmly when reinstalled to avoid erroneous indications due to improper electrical control.

(2) Install top panel with eight screws.

6-10. Front Panel Repair. Perform the following procedure to remove and replace components mounted on the front panel (see figure 6-1 and figure FO-20).

a. Removal. Remove front panel as follows:

(1) Remove six screws securing front panel to frame.

(2) Remove front panel away from cabinet and carefully lay panel on flat surface. Be careful not to put tension on cable harness.

NOTE

To remove and replace front panel components, refer to paragraphs 6-11 through 6-16.

b. Replacement. Replace front panel as follows:

(1) Place front panel in position on cabinet. Be careful not to pinch cable harness wires.

(2) Secure front panel using six screws.

6-11. Rotary Switches Removal and Replacement. Perform the following procedure to remove and replace rotary switch S2 or S3 (see figures 6-1 and FO-20).

a. Removal. Remove rotary switch S2 or S3 as follows:

(1) Remove front panel described in paragraph 6-10a.

(2) Note position of knob pointer, loosen two set screws on switch knob, and remove knob.

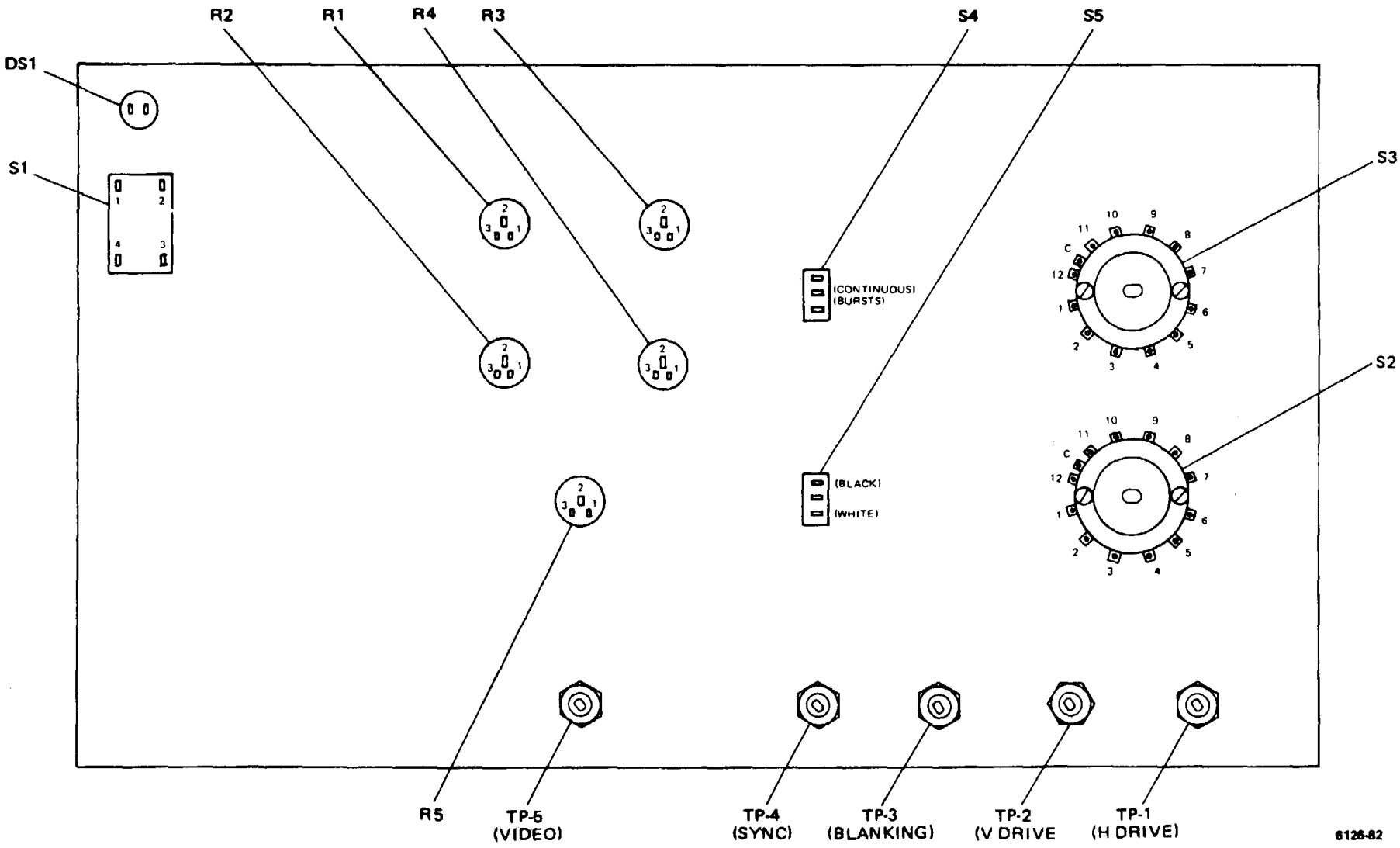


Figure 6-1. Front Panel, Rear View

(3) Tag, unsolder, and remove connecting wires to rotary switch terminals.

(4) Remove nut and lockwasher securing rotary switch to front panel. Observe position of switch terminals and remove switch.

b. Replacement. Replace rotary switch S2 or S3 as follows:

NOTE

When replacing rotary switch S2 (function select), replace diodes CR1 and CR2 between the same switch terminals as the old one (see front panel wiring diagram figure FO-23).

(1) Place lockwasher over switch threads and insert switch through hole in front panel. Position switch as observed in step a. (4).

(2) Secure switch to front panel with nut.

(3) Solder tagged wires to switch terminals.

(4) Position knob on rotary switch (see step a.(2)) and secure with set screws.

(5) Secure front panel to frame described in paragraph 6-10b.

6-12. Toggle Switch Removal and Replacement. Perform the following procedure to remove and replace toggle switch S4 or S5 (see figures 6-1 and FO-20).

a. Removal. Remove toggle switch S4 or S5 as follows:

(1) Remove the front panel described in paragraph 6-10a.

(2) Tag, unsolder, and remove wires to switch terminal.

(3) Remove nut securing switch to front panel and remove switch.

b. Replacement. Replace toggle switch S4 or S5 as follows:

(1) Place nut and lockwasher over switch threads and insert switch through hole is front panel and secure with outside nut. Align switch 90 to the bottom.

(2) Solder tagged wires to switch terminals.

(3) Secure front panel to frame described in paragraph 6-10b.

6-13. Potentiometers Removal and Replacement. Perform the following procedure to remove and replace any potentiometer R1 through R5 (see figures 6-1 and FO-20).

a. Removal. Remove potentiometer as follows:

(1) Remove the front panel described in paragraph 6-10a.

(2) Loosen two set screws on potentiometer knob and remove knob.

(3) Tag, unsolder and remove wires to potentiometer terminals.

(4) Remove nut securing potentiometer to front panel and remove potentiometer.

b. Replacement. Replace potentiometer as follows:

(1) Insert potentiometer through hole in front panel and secure with nut.

(2) Solder tagged wires to potentiometer terminal.

(3) Secure front panel to frame described in paragraph 6-10b

6-14. Test Points Removal and Replacement. Perform the following procedure to remove and replace any test point TP-1 through TP-5 (see figures 6-1 and FO-20).

a. Removal. Remove test point as follows:

(1) Remove the front panel described in paragraph 6-10a.

(2) Unsolder leads to test point and remove nut. Remove test point.

b. Replacement. Replace test point as follows:

(1) Insert test point through hole in front panel and secure with nut.

(2) Solder wires to test point.

(3) Secure front panel to frame described in paragraph 6-10b.

6-15. Power Switch Removal and Replacement. Perform the following procedure to remove and replace power switch (see figures 6-1 and FO-20).

a. Removal. Remove power switch as follows:

(1) Remove the top cover by removing eight screws.

(2) Remove nut securing switch to cabinet and remove switch.

(3) Tag, unsolder, and remove connecting wires to switch.

b. Replacement. Replace power switch as follows:

(1) Solder tagged wires to switch terminals.

(2) Place nut over switch thread and insert switch through hole in cabinet and secure with outside nut.

(3) Replace top cover with eight screws.

6-16. Indicator Lamp Removal and Replacement. Perform the following procedure to remove and replace indicator lamp (DS1) (see figures 6-1 and FO-20).

a. Removal. Remove indicator lamp as follows:

(1) Remove top cover by removing eight screws.

(2) Remove front casing by removing thirteen screws.

(3) Remove sleeving, and then tag, unsolder, and remove connecting wires from indicator lamp.

(4) Remove spring clip securing indicator lamp to cabinet and remove indicator from the front.

b. Replacement. Replace indicator lamp as follows:

(1) Insert indicator lamp through hole in cabinet and secure with spring clip.

(2) Install sleeving over wires, solder wires to indicator, and slide sleeving over terminal connections.

(3) Replace front casing.

(4) Replace top cover with eight screws.

6-17. Rear Panel Repair. Rear panel repair consists of removal and replacement procedures for the power supply components, connectors, and blower. The following paragraphs describe the removal and replacement procedures for these items (see figure 6-2).

6-18. Rear Panel Removal and Replacement. Perform the following procedure to remove and replace the rear panel (see figure 6-2).

a. Removal. Remove rear panel as follows:

(1) Remove the twelve screws securing rear panel.

(2) Remove rear panel away from cabinet. Be careful not to put tension on cable harness.

NOTE

With the rear panel removed, access is provided to remove and replace components mounted on the rear panel and rear cabinet. Refer to paragraphs 6-19 through 6-30 to remove and replace rear panel and cabinet-mounted components.

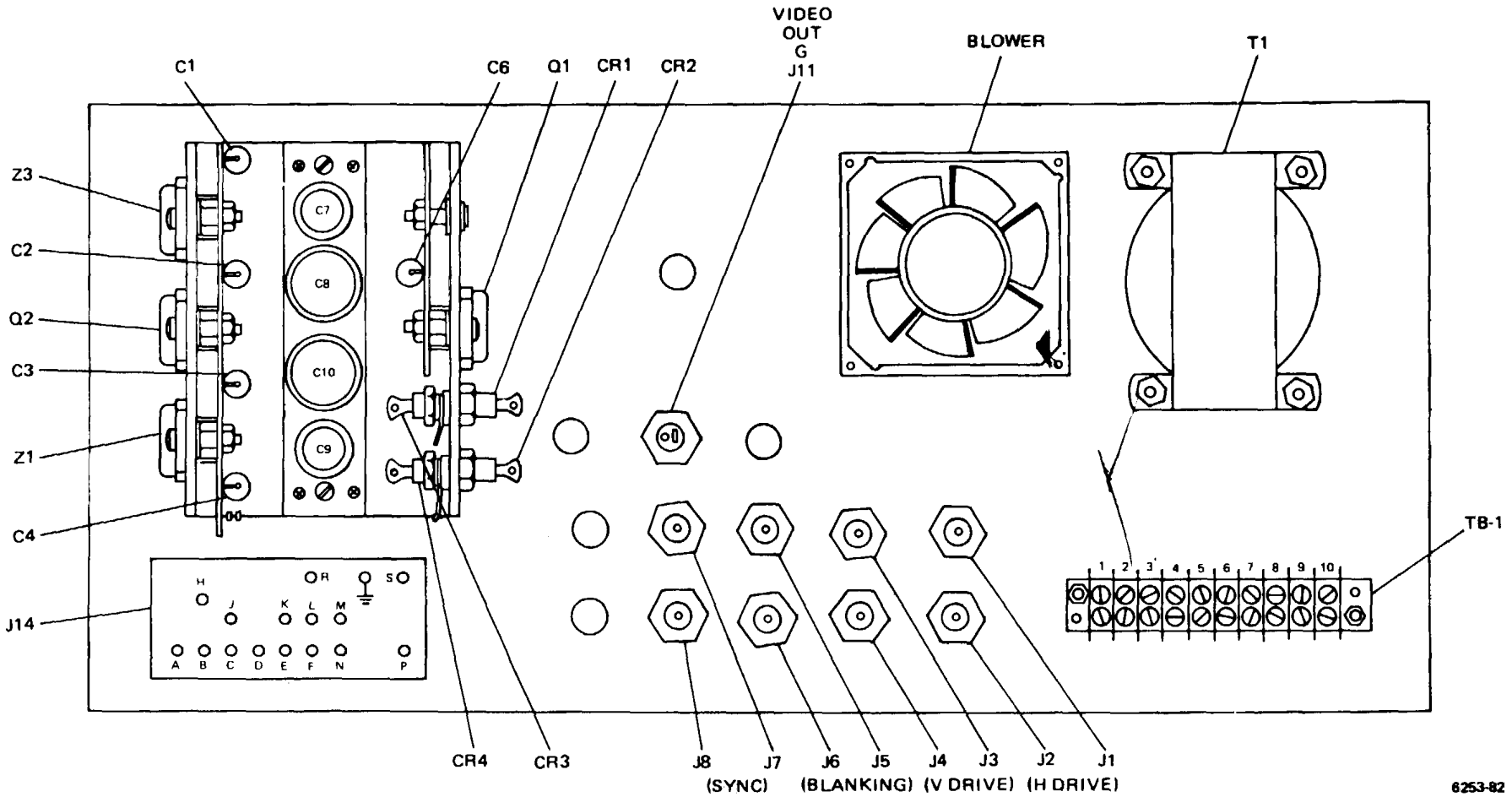


Figure 6-2. Rear Panel Parts Location

b. Replacement. Replace rear panel as follows:

(1) Place the rear panel in position on cabinet. Be careful not to pinch cable harness wires.

(2) Secure rear panel to cabinet with twelve screws.

6-19. Power Transformer. Removal and Replacement. Perform the following procedure to remove and replace transformer (T1) (see figures 6-2 and FO-20).

a. Removal. Remove power transformer as follows:

(1) Remove rear panel described in paragraph 6-18a.

(2) Tag transformer leads on terminal board TB-1. Loosen terminal screws and remove leads (figure 6-2).

(3) Remove four screws on plate covering the transformer mounting screw heads (see figure FO-20).

(4) Remove four screws, lockwashers, flat washers and nuts securing transformer to rear of cabinet. Remove transformer.

b. Replacement. Replace power transformer (T1) as follows:

(1) Install transformer on rear of cabinet and secure with screws, lockwashers, flat washers and nuts.

(2) Secure plate over the transformer mounting screws with four screws.

(3) Connect transformer leads to terminal board.

(4) Install rear panel described in paragraph 6-18b.

6-20. Blower Removal and Replacement. Perform the following procedure to remove and replace blower (see figures 6-2 and FO-20).

a. Removal. Remove blower as follows:

(1) Remove rear panel described in paragraph 6-18a.

(2) Tag blower leads on terminal board TB-1. Loosen terminal screws and remove leads.

(3) Remove four screws and lockwashers securing blower and guard to rear panel.

b. Replacement. Replace blower as follows:

(1) Install blower and guard on rear panel and secure with four screws and lockwashers.

(2) Connect blower leads to TB-1 and tighten screws.

(3) Install rear panel described in paragraph 6-18b.

6-21. Coaxial Connector Removal and Replacement. Perform the following procedure to remove and replace any coaxial connector (see figure 6-2).

a. Removal. Remove coaxial connectors as follows:

(1) Remove rear panel described in paragraph 6-18a.

(2) Tag and unsolder lead(s) to connector.

(3) Remove nut and lockwasher securing connector to rear panel and remove connector.

b. Replacement. Replace connector as follows:

(1) Insert connector into rear panel and secure with nut and lockwasher.

NOTE

Wherever shrink tubing is used, removed tubing must be replaced.

(2) Solder lead(s) to connector.

(3) Install rear panel described in paragraph 6-18b.

6-22. Terminal Board (TB-1) Removal and Replacement. Perform the following procedure to remove and replace terminal board TB-1 (see figure 6-2).

a. Removal. Remove terminal board TB-1 as follows:

(1) Remove rear panel described in paragraph 6-18a.

(2) Tag and disconnect all leads on terminal board.

(3) Remove two screws and lockwashers and nuts securing terminal board to rear cabinet and remove terminal board.

b. Replacement. Replace terminal board TB-1 as follows:

(1) Install terminal board on rear panel and secure with two screws, lockwashers and nuts.

(2) Connect all leads to terminal board and tighten screws.

(3) Install rear panel described in paragraph 6-18b.

6-23. Terminal Board (TB-2) Removal and Replacement. Perform the following procedure to remove and replace terminal board TB-2 (see figure FO-20).

a. Removal. Remove terminal board as follows:

(1) Remove eight screws securing top panel and remove panel.

(2) Tag and disconnect all leads on terminal board.

(3) Remove two screws, lockwashers and nuts securing terminal board to cabinet.

b. Replacement. Replace terminal board TB-2 as follows:

(1) Install terminal board to cabinet case and secure with two screws, lockwashers and nuts.

(2) Connect all leads to terminal board and tighten screws.

(3) Install top panel with eight screws.

6-24. Power Connector/Fuse Holder Removal and Replacement. Perform the following procedure to remove and replace power connector/fuse holder (see figure 6-2).

a. Removal. Remove power connector/fuse holder as follows:

(1) Remove rear panel described in paragraph 6-18a.

(2) Tag and unsolder leads to power connector/fuse holder.

(3) Press spring retaining clips on each end of power connector/fuse holder and remove out from cabinet.

b. Replacement. Replace power connector/fuse holder as follows:

(1) Insert power connector/fuse holder into rear of cabinet until spring retaining clip snaps outward securing power connector/fuse holder to cabinet.

(2) Solder tagged wires to power connector/fuse holder.

(3) Install rear panel described in paragraph 6-18b.

6-25. Heat Sink Filter Assembly Removal and Replacement (see figures 6-2 and FO-22). The heat sink filter assembly consists of heat sink mounted voltage regulators, rectifiers and filter capacitors mounted on the rear of the cabinet. Perform the following procedure to remove and replace the heat sink filter assembly and mounted components.

a. Removal. Remove heat sink filter assembly as follows:

(1) Remove rear panel described in paragraph 6-18a (see figure 6-2).

(2) Remove four screws securing heat sink to rear of cabinet (see figure FO-20).

(3) Remove four flat head screws securing heat sink filter assembly to cabinet.

(4) Tag and unsolder wires connected to heat sink filter assembly and remove.

NOTE

With the heat sink filter assembly removed from the unit, mounted components can be removed and replaced by performing procedures in paragraphs 6-26 through 6-30.

b. Replacement. Replace heat sink filter assembly as follows:

(1) Solder wires to heat sink filter assembly.

(2) Install heat sink filter assembly to cabinet using four flat head screws. Apply silicon thermal compound if required.

(3) Install heat sink to rear of cabinet using four screws. Apply silicon thermal compound if required.

(4) Install rear panel described in paragraph 6-18b.

6-26. Filter Capacitors C7, C8, C9, and C10 Removal and Replacement. Perform the following procedure to remove and replace filter capacitors C7, C8, C9 or C10 (see figure FO-22).

a. Removal. Remove filter capacitor C7, C8, C9 or C10 as follows:

(1) Remove heat sink filter assembly described in paragraph 6-25a.

(2) Remove two screws securing capacitor printed circuit board and lift out circuit board.

(3) Unsolder capacitor leads and remove capacitor from printed circuit board.

b. Replacement. Replace capacitor as follows:

(1) Install capacitor on printed circuit board and solder capacitor.

NOTE

Ensure capacitors are positioned in correct polarity before soldering to printed circuit board.

(2) Secure capacitor circuit board with two screws.

(3) Install heat sink filter assembly described in paragraph 6-25b.

6-27. Filter Capacitor C1 through C6 Removal and Replacement.
Perform the following procedure to remove and replace any capacitor C1 through C6 (see figure FO-22).

a. Removal. Remove any capacitor C1 through C6 as follows:

(1) Remove heat sink filter assembly described in paragraph 6-25a.

(2) Remove filter capacitors circuit board by removing two screws. (This allows access to remove any capacitor C1 through C6.)

(3) Unsolder and remove capacitor.

b. Replacement. Replace any capacitor C1 through C6 as follows:

(1) OBSERVE POLARITY and solder capacitor leads.

(2) Replace filter capacitors circuit board with two screws.

(3) Install heat sink filter assembly described in paragraph 6-25b.

6-28. Rectifiers CR1 through CR4 Removal and Replacement. Perform the following procedure to remove and replace any rectifier CR1 through CR4 (see figure FO-22).

a. Removal. Remove any rectifier CR1 through CR4 as follows:

(1) Remove heat sink filter assembly described in paragraph 6-25a.

(2) Remove two screws securing filter capacitors circuit board. (This will allow access to remove and replace any rectifier CR1 through CR4.)

(3) Unsolder wires connected to rectifier.

(4) Remove nut, wire lug (with wire attached) and insulated washers, and remove rectifier.

b. Replacement. Replace any rectifier CR1 through CR4 as follows:

(1) Install rectifier and secure with insulated washers, wire lug and nut.

(2) Solder wires to rectifier.

(3) Replace filter capacitors circuit board with two screws.

(4) Install heat sink filter assembly described in paragraph 6-25b.

6-29. Power Transistors Q1 and Q2 Removal and Replacement. Perform the following procedure to remove and replace power transistors Q1 and Q2 (see figure FO-22).

a. Removal. Remove power transistor Q1 or Q2 as follows:

(1) Remove heat sink filter assembly described in paragraph 6-25a.

(2) Remove two screws securing filter capacitors circuit board.

(3) Remove two screws, nylon washers, lockwashers, nylon spacers, mica insulator and nuts securing transistor to heat sink and circuit board.

(4) Unsolder transistor terminals connected to circuit board and remove from circuit board and heat sink.

b. Replacement. Replace transistor Q1 and Q2 as follows:

(1) Apply silicon thermal compound to base of transistor.

(2) Insert mica insulator over transistor terminals.

(3) Insert transistor with 2 screws and mica insulator into the holes in heat sink.

(4) Place nylon spacers and washers over screw threads, insert into circuit board and secure with lockwashers and nuts.

(5) Solder transistor terminals to circuit board.

(6) Replace filter capacitors circuit board with two screws.

(7) Install heat sink filter assembly described in paragraph 6-25b.

6-30. Voltage Regulators Z1 and Z3 Removal and Replacement. Perform the following procedure to remove and replace voltage regulators Z1 and Z3 (see figure FO-22).

a. Removal. Remove voltage regulator Z1 or Z3 as follows:

(1) Remove heat sink filter assembly described in paragraph 6-25a.

(2) Remove two screws securing filter capacitors circuit board. (This will allow access to remove and replace voltage regulator Z1 or Z3.)

(3) Remove two screws, nylon washers, lockwashers, nylon spacers, mica insulator and nuts securing voltage regulator to heat sink and circuit board.

(4) Unsolder voltage regulator terminals connected to circuit board and remove regulator from circuit board and heat sink.

b. Replacement. Replace voltage regulator Z1 or Z3 as follows:

(1) Apply silicon thermal compound to base of voltage regulator.

(2) Insert mica insulator over voltage regulator terminals and insert regulator into the two terminal holes in heat sink and circuit board.

(3) Insert regulator with two screws and mica insulator into holes in heat sink.

(4) Place nylon spacers and washers over screw threads, insert into circuit board and secure with lockwashers and nuts.

(5) Solder regular terminals to circuit board.

(6) Replace filter capacitors circuit board with two screws.

(7) Install heat sink filter assembly described in paragraph 6-25b.

6-31. Printed Circuit Board Connectors Removal and Replacement.

Perform the following procedure to remove and replace printed circuit board connectors (see figure FO-20).

a. Removal. Remove printed circuit board connector as follows:

(1) Remove top and bottom panels (eight screws per panel).

(2) Remove printed circuit card (paragraph 6-9a).

(3) Tag and unsolder leads to connector.

(4) Remove two screws, lockwashers and nuts securing connector to card frame and remove connector.

b. Replacement. Replace printed circuit board connector as follows:

(1) Secure connector to frame assembly with two screws, lockwashers and nuts.

(2) Solder leads to connector.

(3) Install printed circuit card (paragraph 6-9b).

(4) Secure top and bottom panels.

6-32. Printed Circuit Card Guide Removal and Replacement. Perform the following procedure to remove and replace card guide.

a. Removal. Remove card guide as follows:

(1) Remove eight screws securing top panel.

(2) Remove printed circuit card (paragraph 6-9a).

(3) Insert the blade of a small flat screwdriver behind the plastic card guide and snap out card guide.

b. Replacement. Replace card guide as follows:

(1) Insert card guide in holes in card frame and push in.

(2) Install printed circuit card (paragraph 6-9b).

(3) Secure top panel with eight screws,

Section V. Performance Verification and Adjustments

6-33. Introduction. The test pattern generator operates automatically, developing an analog television signal through digital techniques. Therefore, no extensive adjustment procedure is required. The procedure outlined in this section should be followed to ascertain that the instrument is functioning properly and that pattern and pulse values are proper for the scan rate in use.

This procedure is dual purpose. It is used to verify performance of the instrument to specification, a procedure which can be accomplished without removal of panels and change of internal controls. If adjustment is desired, as indicated by variations observed during performance verification, the top panel must be removed for access to controls.

6-34. Test Equipment. The performance verifications and adjustment procedures make use of the test equipment specified in the Maintenance Allocation chart in Appendix B.

6-35. Voltage Levels. Power supply levels must be verified prior to performing adjustment procedures (+12v, +5v, and -5v) to establish proper reference levels for all operations. Test points (TP1-TP4) are provided on the power regulator card shown in figure 6-3 to check the voltage levels. Control (R1) is provided at the right side of the power regulator card to adjust the +5v supply. Others are not adjustable.

6-36. Sync Generator Section Adjustment Procedure. Vertical timing is controlled by the counter circuits, and therefore is automatically locked to the horizontal rate.

NOTE

All outputs must be terminated in 75 ohms.

1. Refer to table 6-3 for proper timing relationships for the scan rate in use. See figures 4-1 and 4-4 for conformance to typical waveforms.

2. Sync the oscilloscope from the leading edge (-) of H drive. Set oscilloscope sweep rate as desired for inspection of timing as described in each step of adjustment.

3. Observe the H drive waveform at the rear panel. Pulses should be 8v, pk-pk (unterminated) negative going with edges spaced as shown in table 6-3. Adjust the pulse width to the proper value by use of the control (R1) at the left edge of the drive blanking card (see figure 6-4).

4. Observe the blanking output, with oscilloscope sync remaining at H drive. Observe amplitude, polarity and leading edge spacing shown in table 6-3. Adjust H blanking pulse width by use of the control (R2) second from the left edge of the drive blanking card.

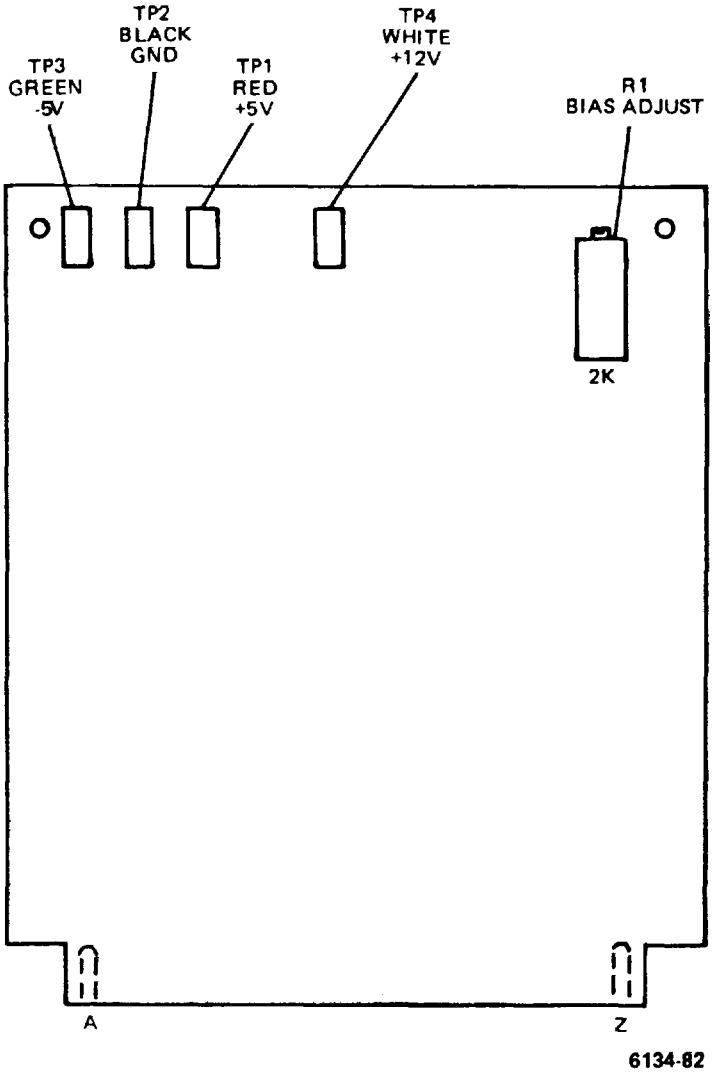


Figure 6-3. Power Regulator Circuit Card Adjustment

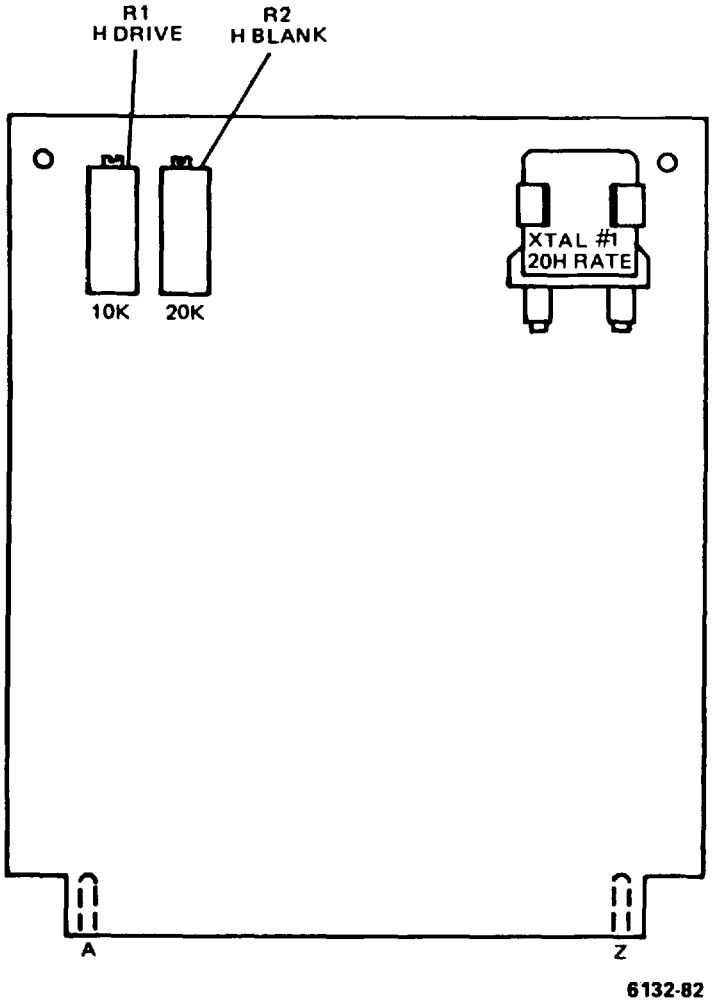


Figure 6-4. Drive/Blanking Circuit Card Adjustments

Table 6-3. Sync Generator Characteristics - 2:1 Interlace

Rate -	
Lines per frame	675
Lines per field	337.5
Field rate	60
2H master oscillator	40.500 kHz
H rep rate	20.250 kHz
Total H line	49.4 usec
Active H line	42.4 usec
Typical pulse widths	
V Drive tv lines	13.5
V Drive porch	3
V Sync	3
V Post	3
V Blanking	26
H Blanking	7.0 usec
H Drive	3.5 usec
H Front porch	1.0 usec
H Sync	2.75 usec
2H Equalizing	1.4 usec
2H Serrations	2.0 usec

NOTES: Pulse widths and rates conform to EIA Standard RS-343.
V blanking nominal pulse width = 1250 usec.
V drive nominal pulse width = 667 usec.

5. Sync the oscilloscope from the leading edge (-) of V drive. Observe the V drive waveform and check polarity, level and width (nominally 667 usec). The pulses should be spaced 16, 667 usec apart, occurring at a 60 Hz rep rate. For 60 Hz field rates, switch oscilloscope sync to line; the pattern should either be stationary or drift very slowly to the right or left. A rapid travel or apparently out of sync signal indicates that the vertical rate is incorrect, due to improper master oscillator frequency or improper line count.

6. Observe the blanking output and check level, polarity and width of the V blanking interval (20 lines, 988 usec at 675 line rate). The H blanking pulses (as adjusted in step 4) should be present at all times except during the V blanking interval. The upper and lower baselines should be uniform with no tilt, sag or modulation.

7. Sync oscilloscope to the leading edge (-) of V drive. Set oscilloscope sweep at 50 usec/div. Observe the sync output and inspect for proper waveform. The sync waveform is presented in the industrial format (figure 4-4) by the selection of jumpers 4 and 6, on the sync card (figure FO-4).

NOTE

If the sync waveform does not appear to be as expected, be sure to check which jumpers are installed on the sync card.

8. Continue to observe the sync output. Sync oscilloscope from the leading edge (-) of H drive, sweeping scope at a convenient rate to show the H sync pulses.

9. Adjust the front porch (leading edge delay) to 1 usec by u3e of control (R6) at the edge of the sync card (figure 6-5). Then adjust the width of the H sync pulse (2.75 usec) by use of control (R16).

10. Adjust the output amplitude (R25) of the output pulses on the pulse output card (figure 6-6) for a nominal level of 4v peak.

6-37. Test Pattern Section Adjustment Procedure.

a. Measurement Conditions.

(1) This procedure is based on the 675/60 scan rate, using pulse widths conforming to EIA Standards as shown in table 6-3.

There is no standard or even common prevailing practice which governs the test requirements or test pattern content for non-broadcast television systems. The adjustment of pattern content is, therefore, somewhat arbitrary and may be set according to system specification requirements or prevailing common practice. In the absence of system standards to the contrary, it is suggested that:

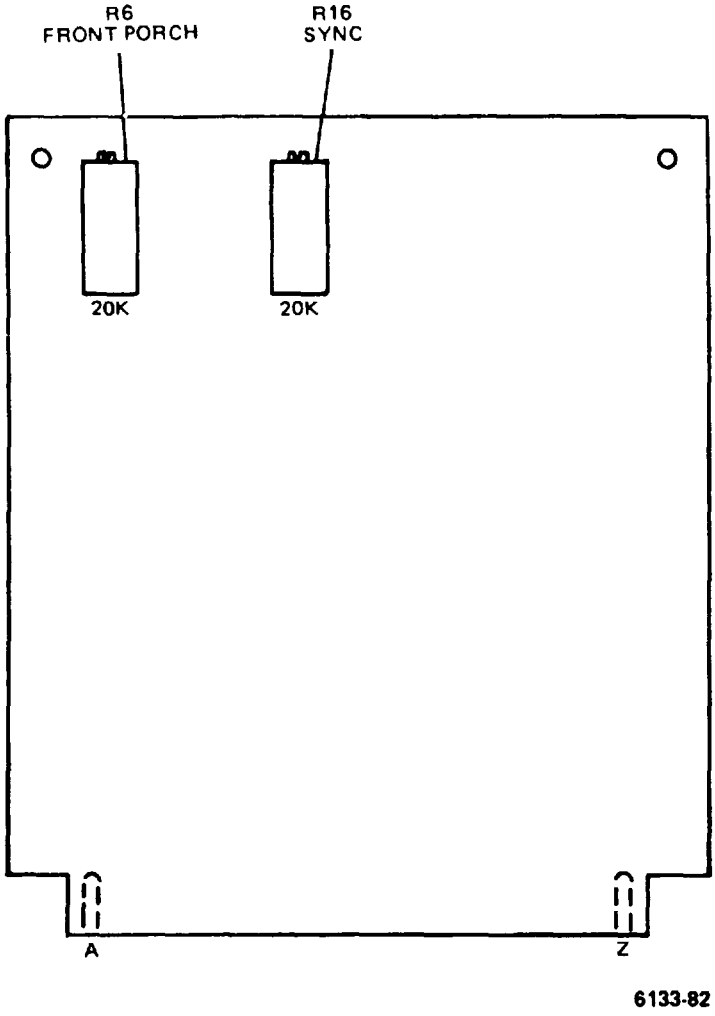


Figure 6-5. Sync Circuit Card Adjustments

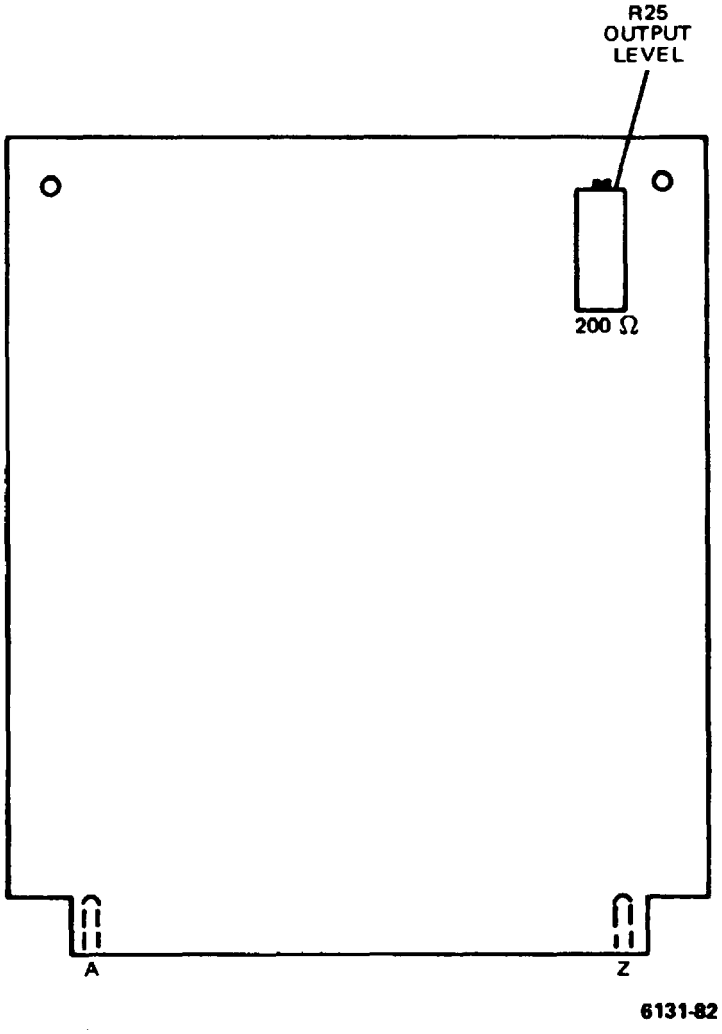


Figure 6-6. Pulse Output Circuit Card Adjustment

(2) Synchronizing pulses conform to EIA Standard RS-343A.

(3) Resolution pattern content be presented in 100 tv line increments. That is, if ten bursts are presented they will be in the order of 100, 200, 300, 400, 500, 600, 700, 800,900 and 1000 tv lines for the scan rate in use.

(4) The window pattern provide a 25% duty cycle. Therefore, the white window pattern would appear as a white rectangle in the center of a black background, the white center covering 25% of the total display area (25% white, 75% black).

(5) The bar/dot patterns be based on 14 vertical and 17 horizontal elements (i.e., 14 H bars and 17 V bars).

(6) The gray scale characteristic should be linear, composed of black, white and eight intermediate shades of gray.

Amplitude and impedance have been outlined in EIA Standards. A 75-ohm system is supplied unless specified otherwise as a modification. Video signal amplitudes may be at one of two common levels:

(7) Video maximum level of 1.0v (including a blanking pedestal of 0.055v) plus sync of 0.4v, making an overall composite video signal of 1.4v pk-pk.

(8) An overall composite video signal of 1.0v, composed of a video maximum level of 0.714v (including a blanking pedestal of 0.4v) plus a sync level of 0.286v.

This instrument normally is adjusted to condition step (7), with a total 1.4v pk-pk composite video signal output. Internal adjustments permit maximum levels as outlined in condition step (8), if desired.

There is no definitive standard on dc condition for video or synchronizing signals in television systems. The video output signal is direct coupled to avoid the slightest tilt in the video frame for some patterns. The blanking level (blacker-than-black) is at approximate ground (zero voltage) with the video portion positive going and sync portion negative going.

Tolerances have not been standardized in the television industry and often vary according to particular system requirements. Therefore, adjustments called out herein are described without specific tolerance range. Pulse width settings are observed upon an oscilloscope display, in which close setting is a matter of technician care in procedure. In factory calibration, a tolerance of $\pm$5% is assumed as a maximum allowance on all oscilloscope measurements i.e., a pulse width of 10 usec must be within $\pm$0.5 usec to be considered acceptable. Pattern content, such as the number of bar elements length of gray scale, etc., is somewhat arbitrary, to be set according to user's judgment as desired in the display of the signal. The scan rate is

often derived from a crystal oscillator, in which case a repetition rate tolerance of 0.01% can be assumed unless specified otherwise. If the line lock mode is used in sync generation, accuracy can be defined only by the stability of the reference power line signal. Synchronizing pulse inputs govern accuracy and stability of the test pattern signal.

b. Adjustment Procedure. The generator is adjusted using an individual procedure for each test pattern, which is complete in itself except the output must be checked first to verify basic signal levels and proportions. For adjustments of all signals, observe the output composite video signal at the video output connector on the rear panel. Refer to circuit ard and control locations, figure FO-21, if adjustments are necessary.

(1) Connect the test pattern generator for use as shown in figure 2-1.

NOTE

If the test pattern generator does not have an internal sync generator accessory, an external source of H drive, V drive, blanking and sync is required. The synchronizing pulse inputs must have proper width and timing of H drive, V drive, sync and blanking pulses for proper calibration at the pattern generator section. Pulse proportions should be as outlined on table 6-3 for the scan rate in use. It is convenient to have H drive and V drive available for oscilloscope sync purposes. If H drive is not available, the oscilloscope could be synchronized from blanking. However this is not as desirable as H drive due to the absence of H blanking pulses during the V blanking interval.

(2) Set oscilloscope channel 1 input amplitude sensitivity at 0.5v per division, direct coupled, unless otherwise stated.

(3) Controls are located on the front panel and on circuit cards inside the unit. The circuit card name and location of the control on the card is given for each control located on a circuit card.

(4) Set oscilloscope sync on external, negative slope (-), ac coupled, unless otherwise noted.

(5) Unless otherwise noted, the video level control at the front panel should be set at 10 (maximum clockwise), output signal at video composite output connector and pattern polarity switch in white position.

(6) The 10 usec per division oscilloscope sweep rate is suggested for 675-line scan rate when observing horizontal information.

(7) The 2 msec per division sweep rate is suggested to observe vertical information for all EIA Standard scan rates and others which have a 60 Hz field rate. The 5 msec per division sweep rate is suggested for vertical television formats having other than a 60 Hz field repetition rate. Be sure that more than a full field is visible on the oscilloscope screen for proper vertical rate pulse inspections.

6-38. Signal Level Adjustments. The level of the video, blanking pedestal and sync portions of the composite video signal output must be verified before inspecting pattern content. Black level, risetime and output impedance must be checked as well. These tests can be conducted even though pattern proportions may not be adjusted to the exact value required.

Amplitude and impedance have been outlined in EIA Standards. Television systems universally are at 75 ohm cable impedance, at the following levels:

Video maximum level of 1.0v (including a blanking pedestal of 0.055v) plus sync of 0.4v, making an overall composite video signal of 1.4v pk-pk.

This test sequence involves the following circuit cards (see figure FO-21):

Video ..... Position 5C
Gray scale control .....Position 5B
Pulse input ..... Position 2C

1 Connect the equipment for test as shown in figure 2-1. Set the oscilloscope sweep speed to 10 usec per division.

2. Connect the oscilloscope external sync to the H drive source. Sync the oscilloscope from the leading (-) edge of H drive.

3. Connect the oscilloscope channel 1 input to the video G composite output connector, properly terminated. Set channel 1 sensitivity at 0.5 per division.

4. Select the WINDOW function, VIDEO LEVEL at 10. Compare the oscilloscope display to figure 6-7a to identify and check level of the video, blanking and sync portions of the signal.

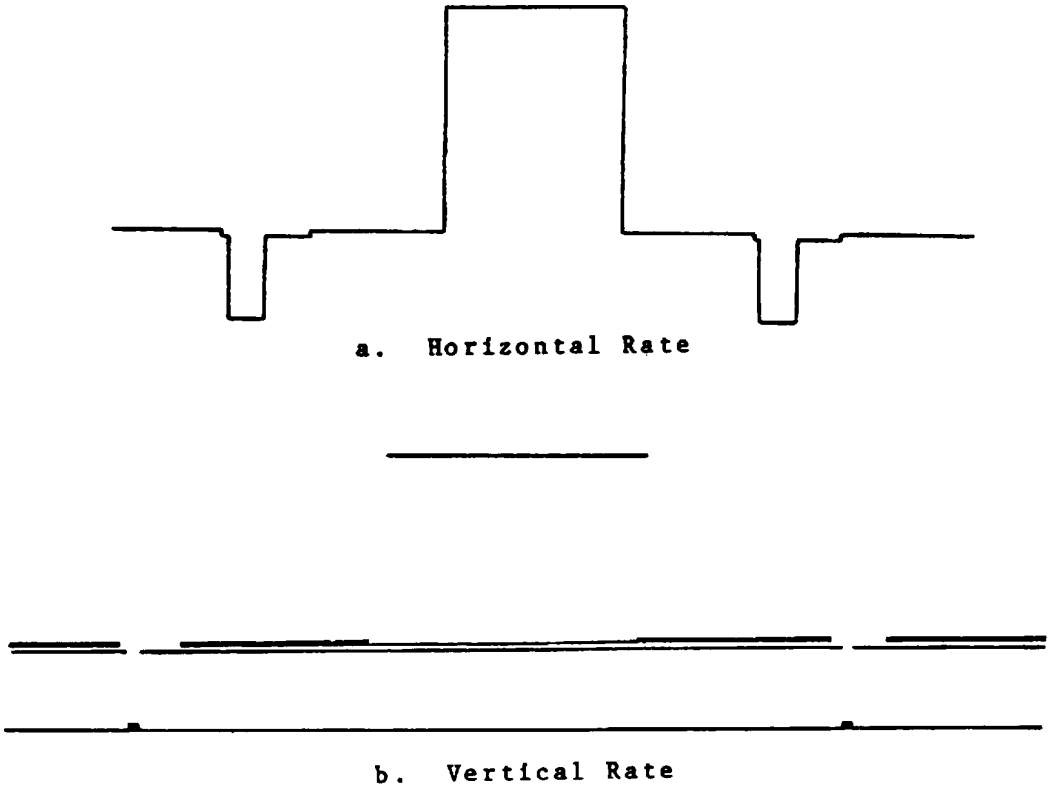


Figure 6-7. Oscilloscope Display of the WINDOW, H STRIPE or V STRIPE Signal Waveform, White Polarity

NOTE

The window offers a low duty cycle test. A central white area is proportioned to provide a 25% duty cycle (average picture level). This is surrounded by a uniform black background over the remainder of the raster. Standard proportions of the white area are 0.50h (50% of the active portion of horizontal line) and 0.50v (50% of the active portion of the vertical field).

The sharp transition from black to white and white to black at the edges of the window in the horizontal dimension provides a convenient tool for analysis of transient response also.

5. Turn the VIDEO LEVEL control to 0. The video portion should no longer be visible except for a slight residual level of the window signal, not exceeding 0.05v. The blanking and sync levels should not have changed.

Black level for other functions must be checked to match the black step of the gray scale.

Select the GRAY SCALE function. While observing the waveform at horizontal rate, VIDEO LEVEL at 10, place the black step (first on the left, to the right of the horizontal blanking interval) at the center of the oscilloscope graticule by use of the oscilloscope horizontal and vertical position control. Make sure oscilloscope input is direct (dc) coupled for this check. Select the V STRIPE function. The black and white levels of video should not shift. If any shift is observed, black level must be adjusted.

6. If adjustment of any signal parameter is indicated, use control R11 of the video card (figure 6-8) to adjust the sync portion of the signal to 0, and using control R46 of the video card, adjust the blanking pedestal to 0. The only signal visible would be the video portion of the gray scale signal.

7 Adjustment of the black level clipper is necessary to match the black level of digitally derived signals to the black level of the gray scale, which is not adjustable. The optimum setting is a compromise at best, and misadjustment can cause signal distortion. Common problems to watch for include:

(a) Black level clipper too low - pedestal will appear higher on bar, dot, window and related signals as compared to the gray scale signal, and the pedestal level will appear to vary as VIDEO LEVEL is turned up and down. The signal will not go completely to zero level as the VIDEO LEVEL control is turned fully counterclockwise to 0.

(b) Black level clipper too high - bottom of gray scale will "push down" into the sync portion of the signal, and it may be necessary to turn the VIDEO LEVEL control clockwise from 0 some amount before the bar, dot, window and related signals will appear from black level. Extreme misadjustment may cause lower steps of the gray scale to be clipped or compressed.

If adjustment is necessary, select gray scale. Turn VIDEO LEVEL to 10 and recheck the vertical position of the black level step on the oscilloscope graticule. Select V STRIPE and observe waveform while adjusting the black level control R18 on the video card. The V stripe black level will shift up and down as the control is turned clockwise and counterclockwise. Carefully adjust it to the point where the black levels are the same, as observed while switching back and forth

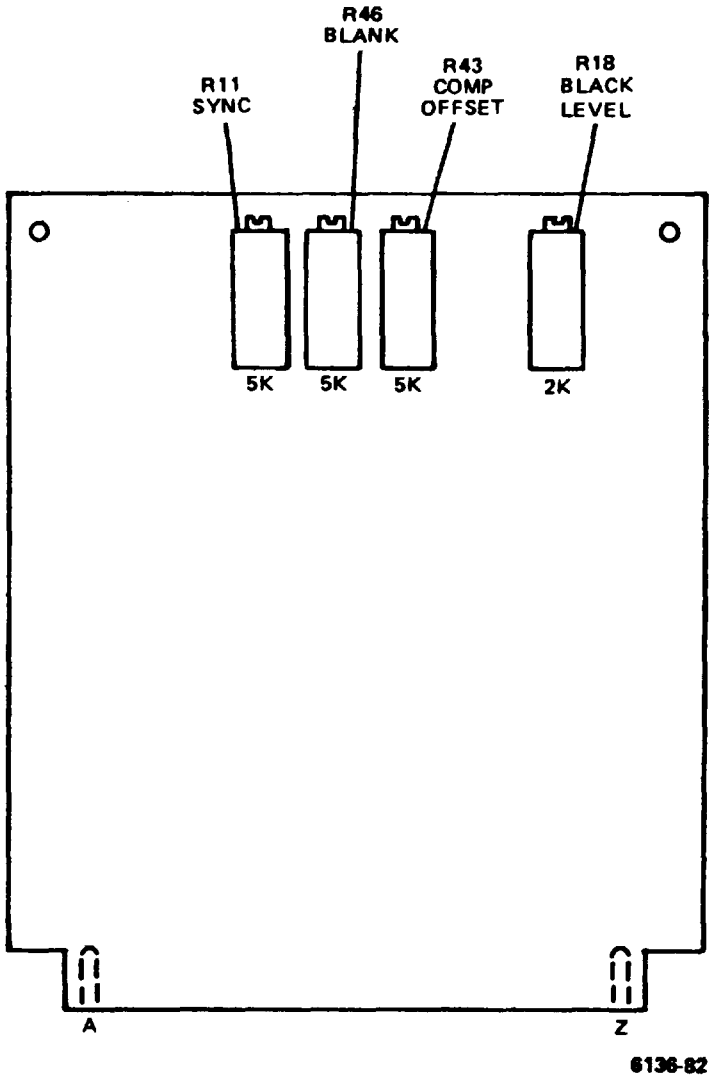


Figure 6-8. Video Circuit Card Adjustments

between the GRAY SCALE and V STRIPE functions. If the control is too high, the black step of the gray scale waveform will be clipped and reduced in height. If it is too low, the V stripe black level will be below the gray scale black level.

8. Return the VIDEO LEVEL control to 0 (maximum counterclockwise). Set the oscilloscope channel 1 input sensitivity at 0.l1 per division. Adjust control (R43 on the video card) counterclockwise to obtain desired blanking pedestal level, nominally 0.055v.

9. Set oscilloscope channel 1 input amplitude sensitivity at 0.5v per division. 6

10 Adjust the sync level control R11 of the video card to set amplitude of the sync portion of the signal at 0.4v peak-to-peak ±0.04v or other desired amplitude.

11. Set front panel VIDEO LEVEL control at 10. Adjust the white level using control.R32 of the gray scale control card (figure 6-9) for 1.0v or other desired limit of video portion of the composite video signal (including 0.055v blanking level). The composite video signal should then be 1.4v (1.0v video with 0.055v and blanking pedestal +0.4v sync).

12. If the levels are to be adjusted for less than maximum values, reduce the amplitudes obtained in steps 8 through 11 as required.

13. To check source impedance, remove the termination at the coax tee on oscilloscope channel 1 input .The signal level should double from those set in steps 8 through 12. Replace the termination.

14. This completes signal level adjustments.

6-39. Flat Field Adjustments. The circuit cards involved in the flat field pattern (see figure FO-21) include:

Video	Position 5C
Pulse Input	Position 2C
Polarity	Position 3C
Gray Scale Control	Position 5B

1. Set oscilloscope sweep rate to 2 msec per division.

2. connect the oscilloscope external sync input to the V drive source.

3. Connect the video coax cable to the video G output connector and oscilloscope channel 1 input. Set oscilloscope channel 1 input amplitude sensitivity at 0.5v per division.

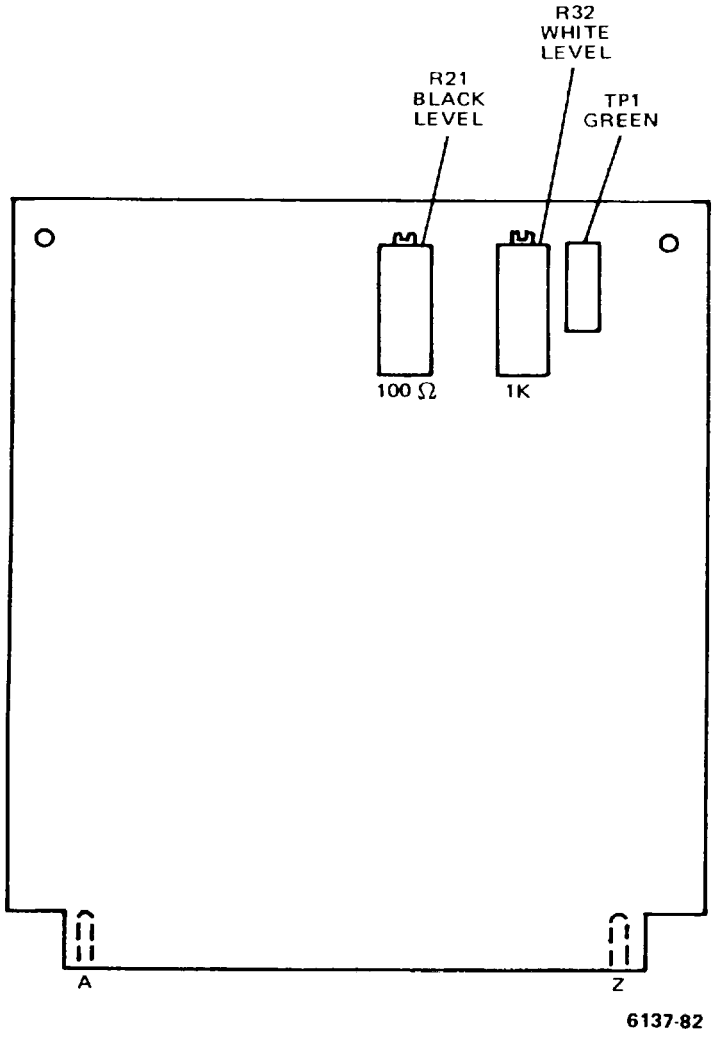
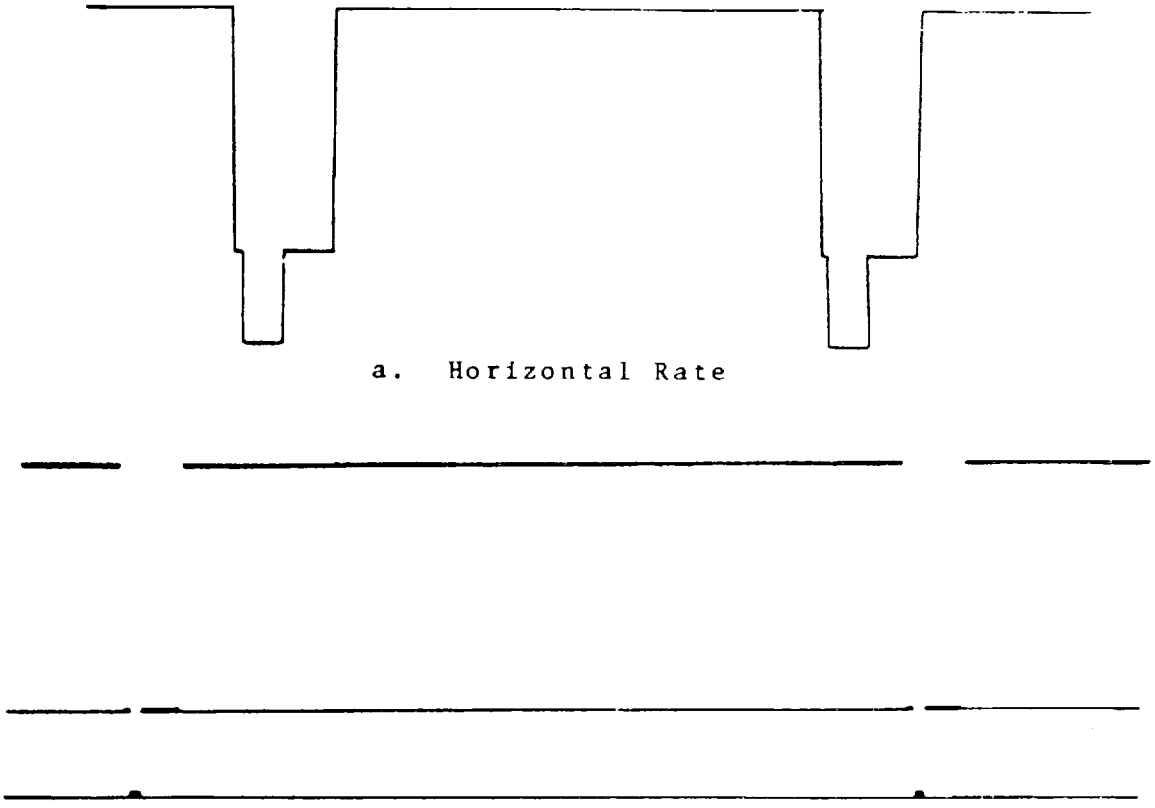


Figure 6-9. Gray Scale Control Circuit Card



a. Horizontal Rate

b. Vertical Rate

Figure 6-10. Oscilloscope Display of the FLAT FIELD Signal Waveform

NOTE

The flat field is an all-white, uniform signal of 100% duty cycle (APL). It represents a maximum load, and the uniform display permits evaluation of undesired brightness modulation which may be introduced into the display by the display device.

4. Set the function selector switch at FLAT FIELD and VIDEO LEVEL at 10. Compare oscilloscope display to figure 6-10b.

5. There are no adjustments for this function. An appearance of difficulty will indicate a need to repeat the signal level adjustments procedure (paragraph 6-35), sync generator calibration procedure, or to perform repairs as indicated.

6. Observe the video portion of the output composite video signal while turning the VIDEO LEVEL control from 0 to 10. Video amplitude should vary from 0.0v to 1.0v peak-to-peak ±0.10v.

7 Connect the oscilloscope external sync output to the H drive source

8 Set oscilloscope sweep to view horizontal information.

9. Compare oscilloscope display to figure 6-10a.

10 Connect the video output connector to the monitor input. The flat white pattern should be obtained with no visible hum or interference.

11. Performance verification of the flat field function is now complete.

6-40. V Bar, H Bar, Bar and Dot Adjustments. The V bar, H bar, bar and dot patterns are related and are derived from common horizontal and vertical elements. Therefore, adjustment is considered for the total group of patterns. The circuit cards involved include (see figure FO-21):

V bar	Position 1B
H bar	Position 2B
Polarity	Position 3C

a. V Bar.

(1) Connect oscilloscope channel 1 input to the video G output connector at the rear panel.

(2) Set oscilloscope sweep rate to 10 usec per division.

(3) Set the oscilloscope channel 1 input amplitude sensitivity at 0.5v per division

(4) Connect the oscilloscope external sync connector to the H drive source.

(5) Set the function selector switch at V BAR.

(6) Compare oscilloscope display to figure 6-11a. Nominal setting is 17 V bar elements for whatever scan rate is in use.

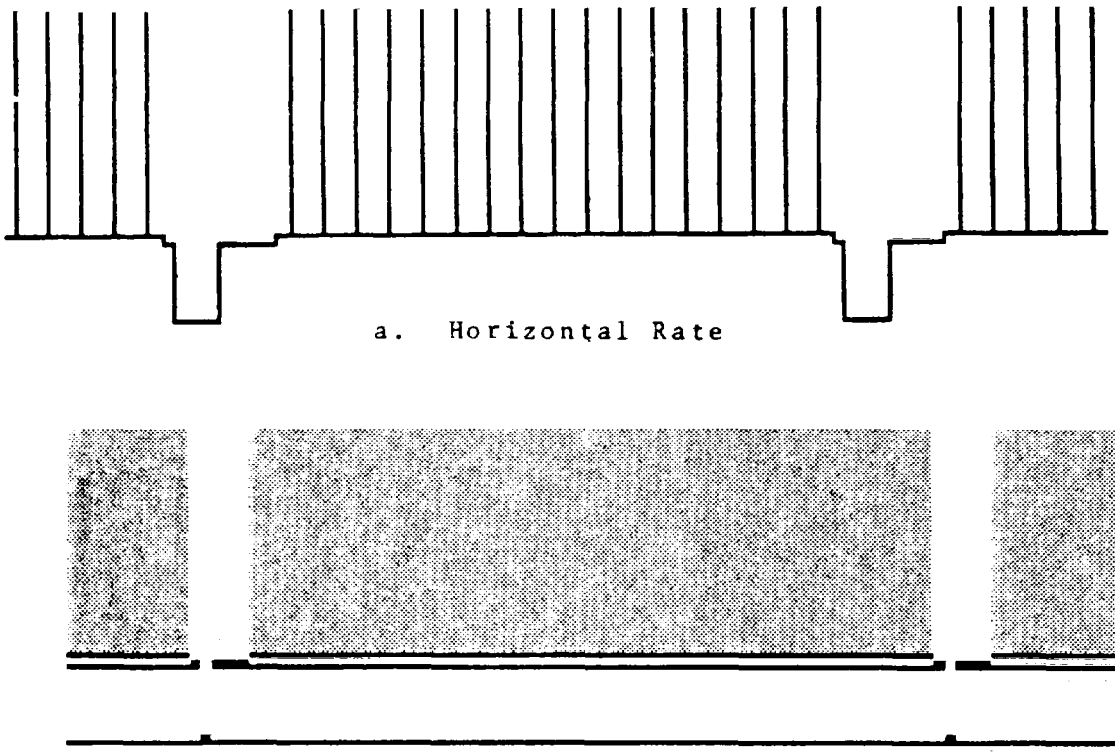


Figure 6-11. Oscilloscope Display of the V BAR Signal Waveform, White Polarity

NOTE

Adjustment of the V bar is complicated by the fact that current standards do not provide a constant percentage of inactive blanking time for the various scan rates. Therefore, adjustment must be based upon the active time of the television scanning line only. Based upon the 525-line, 4:3 aspect ratio precedent, calibration for this rate provides element spacing of 1/20 total line time, or 3.17 usec, between elements. Referred to the nominal active time, elements occur at intervals of 0.0605t (t = active line time). Therefore, the calibration of width between adjacent V bars shall be based upon 0.0605 times the active line duration for all scan rates, providing 17 visible bars in the length of as canning line for the 4 x 3 aspect ratio of 0.071t for the 1 x 1 aspect ratio.

(7) Set the controls to display the number of elements desired in the position desired. The position of the V bar elements is variable by use of the H position control at the front panel. Check that the control range changes position in the pattern slightly more than a distance equal to the width between elements at all settings of the HSPACING control Leave the H position control set at mid-range, because this control will vary the number of V

(8) The number of V bar elements generated in the horizontal tv line is variable by use of the H SPACING control at the front panel. Check control range. The number of elements displayed will depend on the scan rate being used because the length of horizontal line is different for various scan rates. At the 675-line rate, typical range is from 5 to 35 elements.

(9) Set oscilloscope B delayed sweep to 0.1 usec per division and adjust the sweep delay time to show one dot element .Adjust the size of the V bar elements with the V bar size control (R25 on the V bar card, figure 6-12). This also adjusts the size of the dot elements in the dot pattern. Set the control to obtain V bar element width at 0.10 usec pulse width $\pm$0.05 usec. Return oscilloscope to A sweep (undelayed) .

(10) Set pattern switch to BLACK. Set oscilloscope sweep to 2 msec. Compare oscilloscope display to figure 6-13. Return pattern switch to WHITE.

(11) Observe the video portion of the signal while turning the VIDEO LEVEL control from 0 to 10. Video amplitude should vary from 0.0v to 1.0v peak-to-peak $\pm$0.10v. The sync and blanking portions of the composite video signal should remain at the levels set in flat field.

(12) Set oscilloscope sweep to 2 msec. Connect the oscilloscope external sync to the V drive source. Compare oscilloscope display to figure 6-11b.

(13) Connect the video G connector to the monitor input to view the V bar pattern. Check that the V bars are straight, a white pattern on a black background. Select BLACK pattern, which should provide a black V bar pattern on a white background. Return pattern switch to WHITE.

(14) Performance verification of the V bar function is now complete.

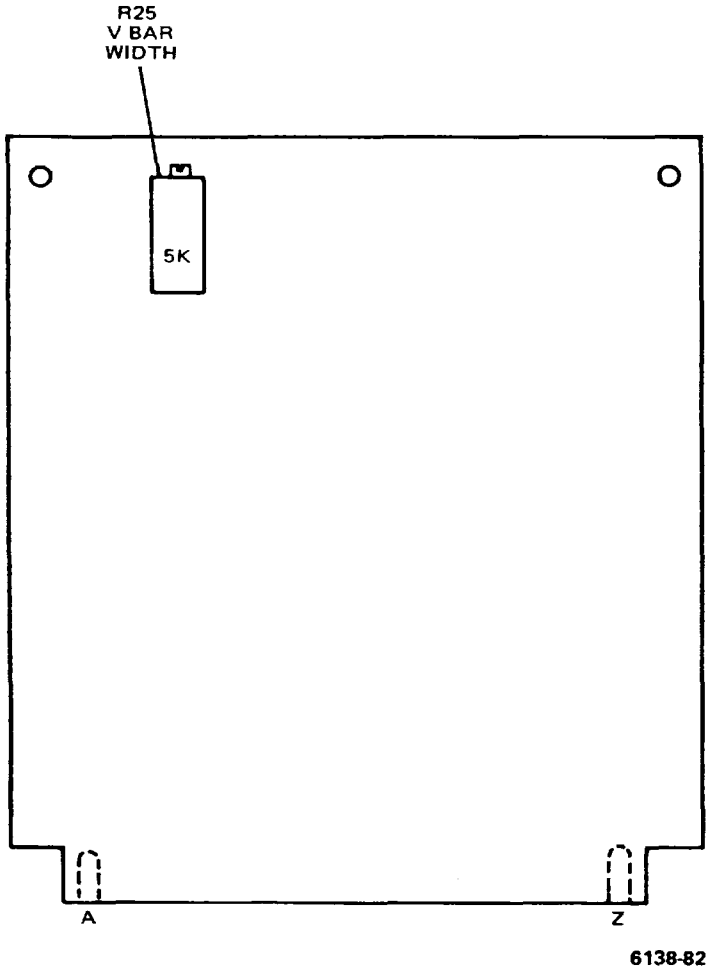


Figure 6-12. V BAR Circuit Card Adjustments

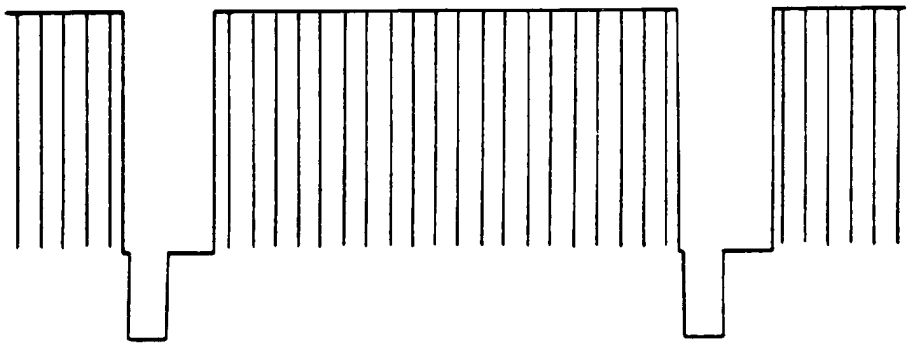


Figure 6-13. Oscilloscope Display of the Typical V BAR Signal Waveform at Horizontal Rate, Black Polarity

b. H Bar.

(1) Connect the oscilloscope channel 1 input to the video G output connector at the rear panel

(2) Set oscilloscope sweep rate to 2 msec.

(3) Set oscilloscope channel 1 input amplitude sensitivity at 0.5v per division.

(4) Connect oscilloscope external sync input to the V drive source.

(5) Set the function selector switch at H BAR.

(6) Compare the oscilloscope display to figure 6-14. Nominal setting is 14 H bar elements in the television field.

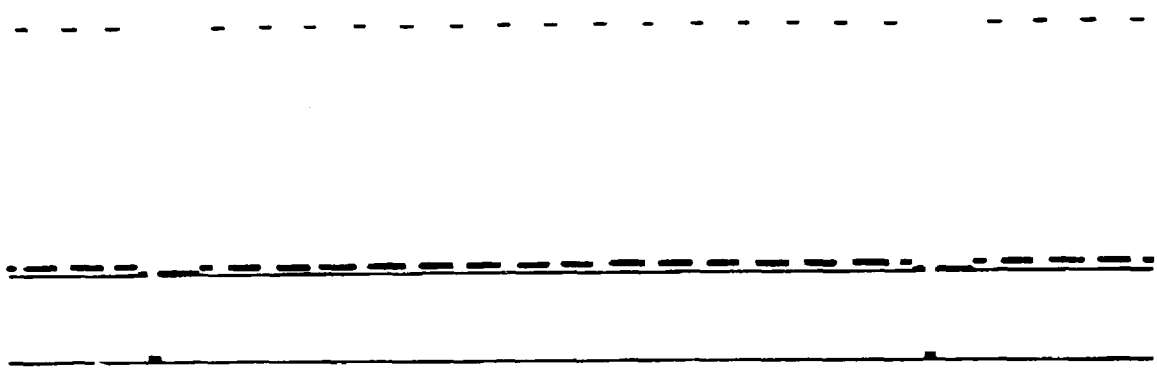


Figure 6-14. Oscilloscope Display of the H BAR signal Waveform at Vertical Rate, White Polarity

NOTE

Adjustment of the H bar elements in the vertical plane of the pattern is based upon 15 elements spaced equally in the total vertical television field, including blanking time. The vertical field is produced at 60 Hz for all scan rates described by present U.S. EIA Standards; therefore, the repetition rate for H bar elements is 900 Hz, requiring 1,111 usec between the elements. One of the 15 elements will occur within the vertical blanking interval and will not be visible. For practical purposes, the pattern is composed of 14 the vertical plane of the active raster. Considering the exact amount of the raster obscured by vertical blanking, it is necessary to generate 13.88 intervals between H bars, each interval 1,111 usec.

It is necessary, in an accurately generated pattern, for the H bar element to occur for one complete scan line, positively locked so as to preclude drift or "run through" that will permit intensification of partial lines, etc. Otherwise, an error of at least one scan line width can occur in the display of the pattern.

These factors present a conflict; 1,111 usec is not an even multiple of the scanning line time for any of the EIA Standard scan rates. Therefore, it is necessary to accept a compromise in internal timing. The vertical interval between H bars is allowed to vary. This provides the desired visible 14 elements of H bar, slightly off the 15th multiple of vertical field rate.

(7) The position of the H bar elements is variable by use of the V POSITION control on the front panel. Check that the control range changes position of the pattern slightly more than a distance equal to the width between elements at all settings in the V SPACING control. Leave the V POSITION control set at mid-range, because this control will vary the number of V bar elements since some elements may be moved off the display when position is adjusted.

(8) The number of H bar elements generated in the vertical tv field is variable by use of the V SPACING control at the front panel. Check that the control range provides a minimum of 10 or less elements and a maximum of 18 or more elements. Most common scan rates include the same field and frame rates, 60 and 30 Hz respectively. Therefore, the number of H bar elements will be the same for many scan rates. Set the control to display the number of H bar elements desired in the positions desired.

(9) Observe the video portion of the signal while turning the VIDEO LEVEL control from 0 to 10. Video amplitude should vary from 0.0v to 1.0v peak-to-peak $\pm$0.10v. The sync and blanking portions of the composite video signal should remain at the levels set in flat field.

(10) Set pattern switch to BLACK. Set oscilloscope sweep to 2 msec per division. Connect the oscilloscope external sync input to V drive source. Compare oscilloscope display to figure 6-15. Return pattern switch to WHITE.

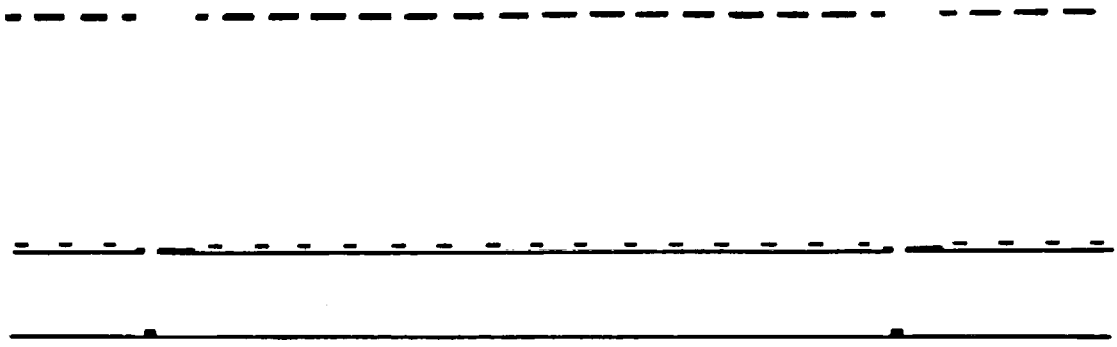


Figure 6-15. Oscilloscope Display of the Typical H BAR Signal Waveform at Vertical Rate, Black Polarity

NOTE

This instrument provides the pattern in either white polarity or black polarity, as selected at the front panel. White polarity provides a white pattern element on a black background, as shown in figures 6-11 and 6-14. A black element developed on a white background is generated in the black polarity, as shown above. Signal timing and calibration is the same in either instance.

(11) Connect the video output connector to the monitor input to display the H bar pattern. Check that H bars are straight. Check that when the pattern control is set on BLACK, black bars on a white background are obtained and when the pattern control is set on WHITE, white bars on a black background are obtained.

(12) Performance verification of the H bar function is now complete.

c. Bar.

(1) Connect the oscilloscope channel 1 input to the video output connector at the rear panel.

(2) Set the oscilloscope sweep to 2 msec per division.

(3) Connect oscilloscope external sync to the V drive source.

(4) Set the function selector switch at BARS.

(5) Compare oscilloscope display to figure 6-16.

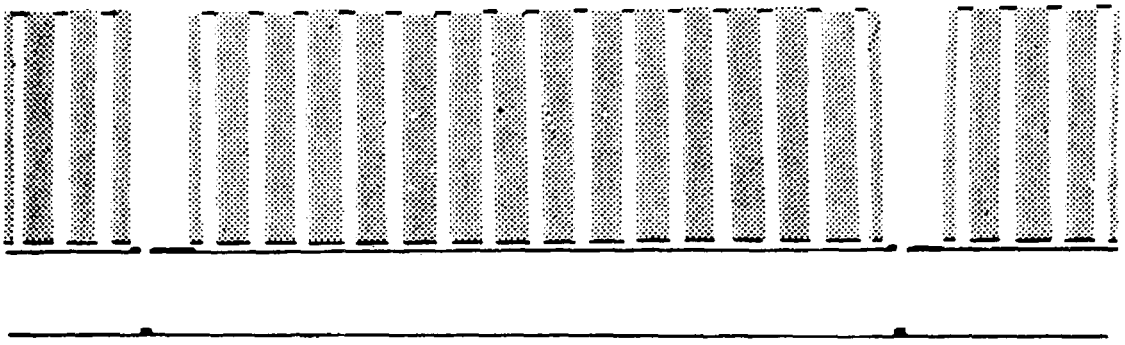


Figure 6-16. Oscilloscope Display of the BAR signal Waveform at vertical Rate, White Polarity

NOTE

Inasmuch as the bar pattern is composed of the H bar and V bar elements, it is not necessary to provide a separate adjustment procedure for this pattern. The dot pattern provides a small dot of brightness at the points on the display at which the V bar and H bar elements intersect in the bar pattern, and therefore are located by H bar and V bar adjustment.

(6) Adjustment of the vertical elements in the bar pattern is set by adjustment of the V bar pattern; refer to V bar adjustment for proper control settings. Check that width and position control ranges continue to be the same for the bar signal.

(7) Adjustment of the horizontal elements in the bar pattern is set by adjustment of the H bar pattern; refer to H bar adjustment for proper control settings. Check that the width and position control ranges continue to be the same for the bar signal.

(8) Observe the video portion of the signal while turning the VIDEO LEVEL control from 0 to 10. Video amplitude should vary from 0.0v to l.0v peak-to-peak $\pm$0.10v. The sync and blanking portions of the composite video signal should remain at the levels set in flat field adjustment

(9) Connect the video output connector to the monitor input to display the bar pattern. Trim the V bar element size to match the H bar element size, if desired, using the control on the V bar card. (See para. 6-40a; step 9 of V bar.)

(10) Check that the pattern control is set on BLACK, black bars on a white background are obtained, and when pattern control is set on WHITE, white bars on a black background are obtained.

(11) Performance verification of the bar function is now complete.

d. Dot.

(1) All adjustments of the position and proportion of the dot pattern are determined by the adjustments made to the bar pattern, for dots are generated at the intersection of the H and V elements in the bar pattern. Dot size is adjustable as outlined under V bar adjustment.

(2) Set the function selector switch on DOT.

(3) Connect oscilloscope channel 1 input to the video output connector at the rear panel.

(4) Set the oscilloscope sweep rate. Connect oscilloscope external sync connector to the V drive source. Set oscilloscope channel 1 input amplitude sensitivity at 0.5v per division.

(5) Compare oscilloscope display to figure 6-17.

(6) Observe the video portion of the signal while turning the VIDEO LEVEL control from 0 to 10. Video amplitude should vary from 0v. to 1.0v peak-to-peak $\pm$0.10v. The sync and blanking portions of the composite video signal should remain at the levels set in flat field.

(7) Connect the video output connector to the monitor input to display the dot pattern. Check that dots occur at the intersection of the H bar and V bar elements of the bar pattern. The white dots are displayed on a black background for the WHITE pattern mode, and the black dots are displayed on a white background for the BLACK pattern mode.

(8) Performance verification of the dot function is now complete.

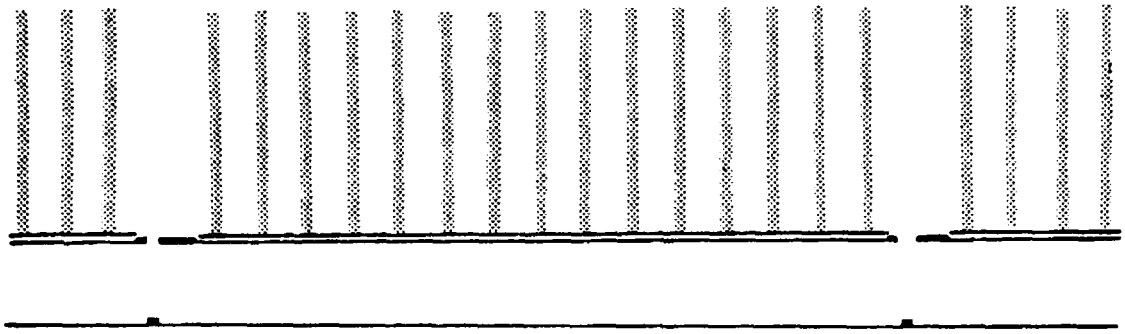


Figure 6-17. Oscilloscope Display of the DOT Signal Waveform at Vertical Rate, White Polarity

6-41. H Stripe, V Stripe, and Window Adjustments. These patterns are related and are derived from common horizontal and vertical elements. Therefore adjustment is considered for these patterns as a group. The circuit cards involved include (see figure FO-21):

H Window.....Position 3B
V Window.....Position 4B
Polarity ..... Position 3C

a. V Stripe.

(1) Set the oscilloscope sweep speed to 10 usec per division

(2) Connect oscilloscope external sync to the H drive source

(3) Set the function selector on V STRIPE and pattern switch to WHITE.

(4) Connect oscilloscope channel 1 input to the video G output connector at the rear panel.

(5) Compare oscilloscope display to figure 6-7a.

(6) The adjustment range allows the V stripe to be shifted and adjusted in size as desired from left to right to extremes which will cut off part of the pattern on the left, and in the right to an extreme which will cause the V stripe to be developed in every other line, resulting in a striped flickering effect rather than the normal display. This pattern should be adjusted so that the entire V stripe is shown in the center area of the raster. Refer to figure 6-7a.

(7) Adjust left margin 25% of the active line time (10.6 usec $\pm$0.1 usec at the 675-line rate) using the H position control 38 located on the H WINDOW card (figure 6-18).

(8) The H width control should vary the horizontal width of the V stripe from approximately 7.0 usec at minimum range to 39 used at maximum range. Adjust the horizontal spacing of the V stripe to 50% of active line time (21.2 usec $\pm$0.1 usec at 675-line rate) using the H width control R39 located on the H WINDOW card.

(9) The width of the right margin should be the same as the left margin, 25% of the active line time (10.6 usec $\pm$0.1 usec).

(10) Set pattern switch to BLACK and compare to figure 6-19a. Return pattern switch to WHITE.

(11) Observe the video portion of the signal while turning the VIDEO LEVEL control from 0 to 10. Video amplitude should vary from 0.0v to 1.0v peak-to-peak $\pm$0.10v. The sync and blanking portions of the composite video signal should remain at the levels set in signal level adjustments (paragraph 6-38).

(12) Connect the video G output connector to the monitor input to display the V stripe pattern. Check that when the pattern control is set on WHITE, a white stripe covering 50% of the width of the raster is obtained at the center of the raster, and when the pattern control is on BLACK, a black stripe of the same proportion is obtained

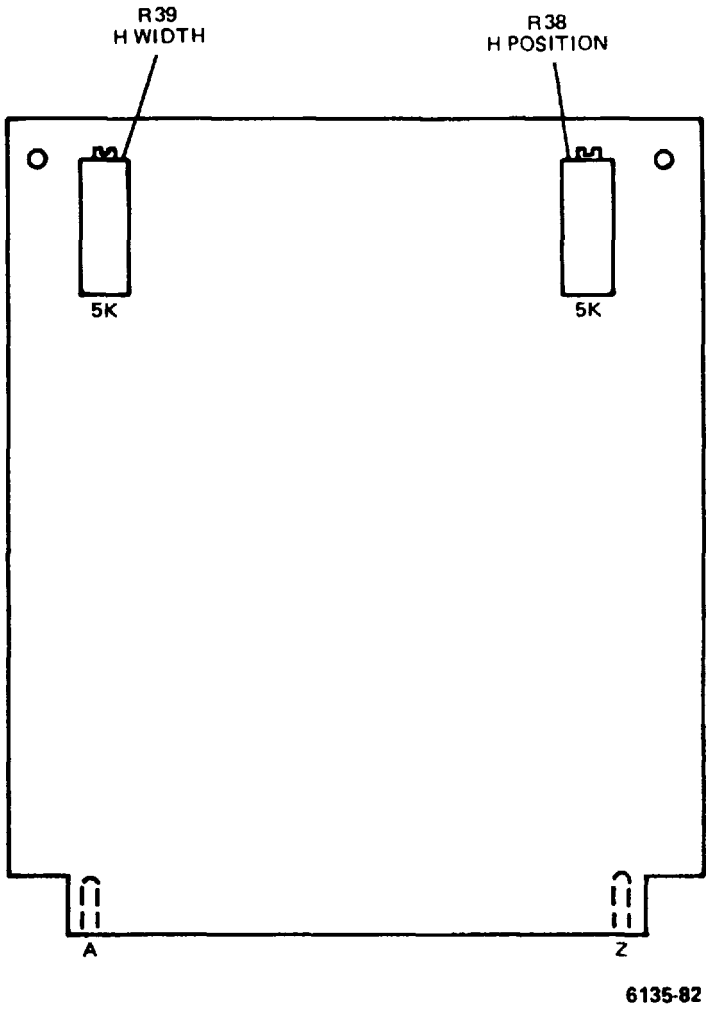


Figure 6-18. H WINDOW Circuit Card Adjustments

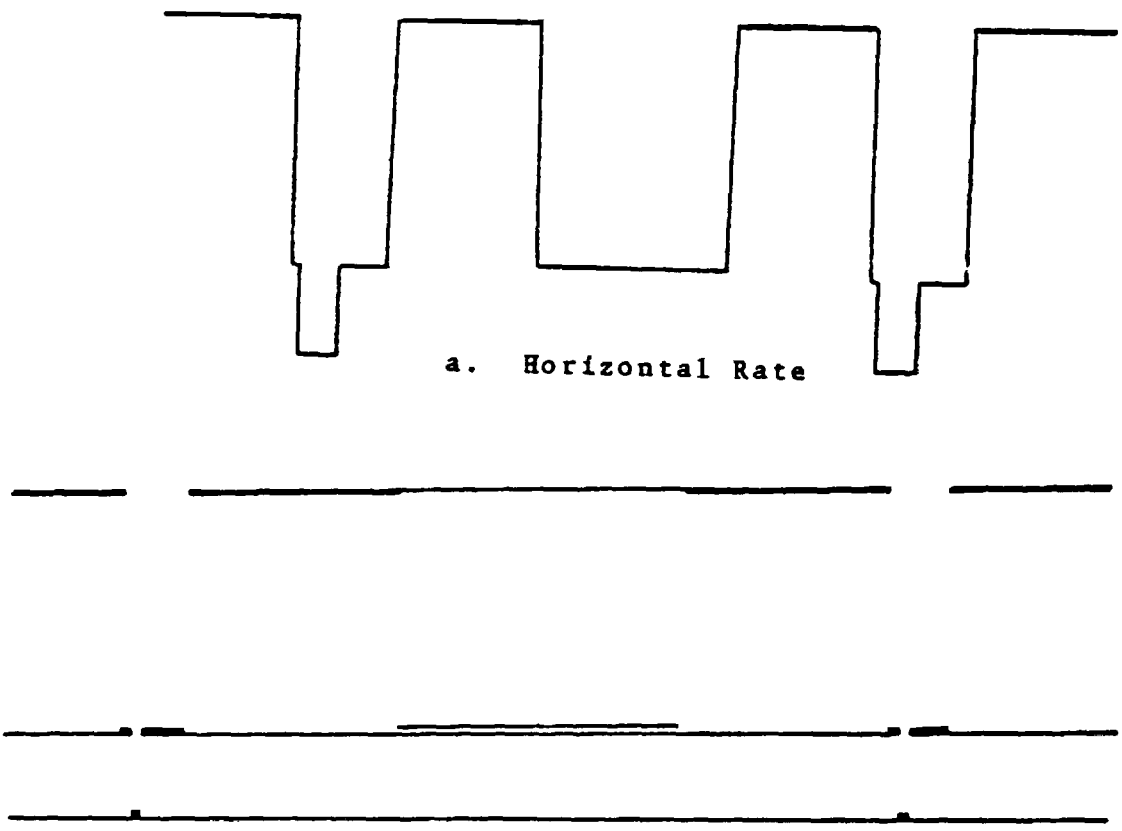


Figure 6-19. Oscilloscope Display of the WINDOW, Signal Waveform, Black Polarity

NOTE

V Stripe

The horizontal component of the window signal presented for the full duration of the vertical television field will develop a vertical stripe on the televised display. This will provide an approximate 50% duty cycle (APL),thus preventing the development of distortion which may be present during the lower APL of the window signal. Therefore the transient response and midfrequency response can be evaluated without distortion due to low frequency defects.

H Stripe

The vertical component of the window signal presented for the full duration of the horizontal television line will develop a horizontal stripe on the television display. This will provide an approximate 50% duty cycle (APL), forming a field rate square wave, ideal for clamp and dc restorer tests under typical operating conditions.

(13) Performance verification of the V stripe function is now complete.

b. H Stripe.

(1) Set the oscilloscope sweep speed to 2 msec per division

(2) Connect oscilloscope external sync to the V drive source.

(3) Set function selector to H STRIPE, and pattern switch to WHITE.

(4) Compare oscilloscope display to figure 6-7b.

(5) The adjustment range allows the H stripe to be shifted as desired from top to bottom extremes which will cut off part of the pattern at the top and on the bottom to an extreme which will cause the H stripe to be developed in every other field resulting in a striped flickering effect rather than the normal display. This pattern should be adjusted so that the entire pattern is shown in the center of the raster.

(6) Adjust the top margin (left on oscilloscope display) to 25% of the active raster (3.85 msec $\pm$0.25 msec) using the V position control (R56) located on the V WINDOW card (figure 6-20).

(7) Adjust the vertical component (center area) of the H stripe pattern to 7.7 msec $\pm$0.5 msec using the V width control (R57) located on the V WINDOW card.

(8) The width of the bottom margin should be the same as the top margin, 25% of the active raster (3.85 msec $\pm$0.25 msec)

(9) Set pattern switch to BLACK, and compare oscilloscope display to figure 6-19b. Return pattern switch to WHITE.

(10) Observe the video portion of the signal while turning the VIDEO LEVEL control from 0 to 10. Video amplitude should vary from 0.0v to 1.0v peak-to-peak $\pm$0.10v. The sync and blanking portions of the composite video signal should remain at the levels set in signal level adjustments (paragraph 6-38).

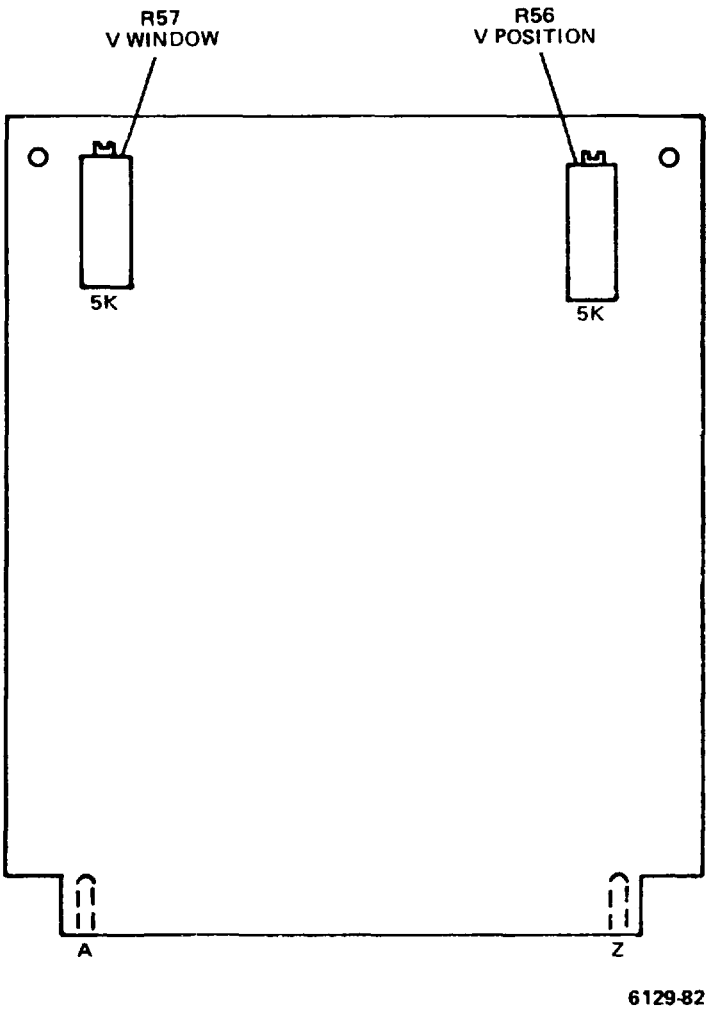


Figure 6-20. V WINDOW Circuit Card Adjustments

(11) Connect the video G output connector to the monitor input to display the H stripe pattern. Check that when the pattern control is on WHITE, a white stripe covering 50% of the height of the raster is obtained at the center of the raster, and when the pattern control is on BLACK, a black stripe of the same proportion is obtained.

(12) Adjustment of the H stripe function is now complete

c. Window.

(1) Select the WINDOW function

(2) The window pattern is a combination of the V stripe and H stripe signals, adjusted by the V stripe and H stripe procedures.

(3) Observe the video portion of the signal while turning the VIDEO LEVEL control from 0 to 10. Video amplitude should vary from 0.0v to 1.0v peak-to-peak ±0.10v. The sync and blanking portions of the composite video signal should remain at the levels set in signal level adjustments (paragraph 6-38).

(4) Connect the video output connector to the monitor input to display the window pattern. Set LEVEL on 10 or other desired level other than 0. A white window on black background with straight edges and no distortion covering 25% of the raster area should be obtained. Check that when the pattern control is set on BLACK, a black window on white background is obtained, and that when the pattern control is set on WHITE, a white window on a black background is obtained.

(5) Performance of the window function is now complete.

6-42. Gray Scale Adjustment. This function develops a gray scale pattern of ascending (rising) slope. The ten step scale (black, eight intermediate gray levels, and white) can be adjusted to provide the most usual linear "stairstep" pattern, or logarithmic or other slope characteristic. The circuit cards involved include (figure FO-21):

Gray scale control .....Position 5B
Gray scale .....Position 6B

1 Set function selector switch at GRAY SCALE.

2 Connect the oscilloscope channel 1 input to the video G output connector at the front panel

3 Connect the oscilloscope external sync input to the H drive source.

4. Oscilloscope sweep rate should show the entire horizontal line when using horizontal related sync and observations. Set oscilloscope channel 1 input amplitude sensitivity at 0.5v per division.

5. Compare the oscilloscope display to figure 6-21A.

6. The length of scanning line in which the gray scale is presented, is adjusted by using the control R1, (step 1) located on the GRAY SCALE CONTROL card, figure 6-22. This should be adjusted if the gray scale does not extend across the horizontal line which would show a large margin of white at the right side of the display or if the gray scale is incomplete through the horizontal line period.

7. Check that there is a proper staircase presentation with steps of correct proportion. If there is any deviation from this figure, adjustment should be performed as outlined below. The procedure is written for generation of a linear gray scale; if other than a linear stairstep presentation is desired, a procedure should be followed which will obtain that presentation.

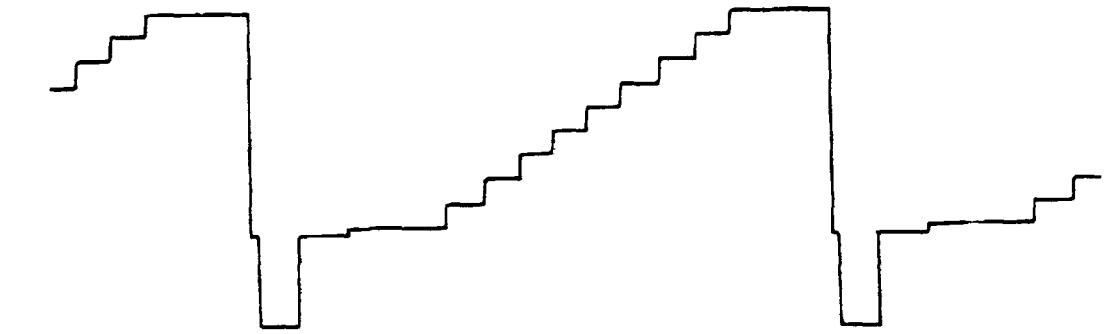
8. Using the VIDEO LEVEL control, adjust the black-to-white video amplitude (not including the blanking pedestal) to 0.9v peak-to-peak when properly terminated.

9. Starting with the control R8 on the GRAY SCALE card, adjust the level of the top step of the gray scale down from white by 0.1v. Using the next control (R7) on this card, adjust the second step 0.1v down from the previous step. Moving to the next control (R6), adjust the third step and then the fourth step using the next control (R5) on the card. In the same manner, adjust all controls on the GRAY SCALE card until all eight steps between black and white have been adjusted to 0.1v. The horizontal and vertical positions of the oscilloscope display may be shifted to place the step under adjustment at the center graticule lines for convenience in adjustment of the gray scale levels. There should be gray scale at each minor division for a linear gray scale.

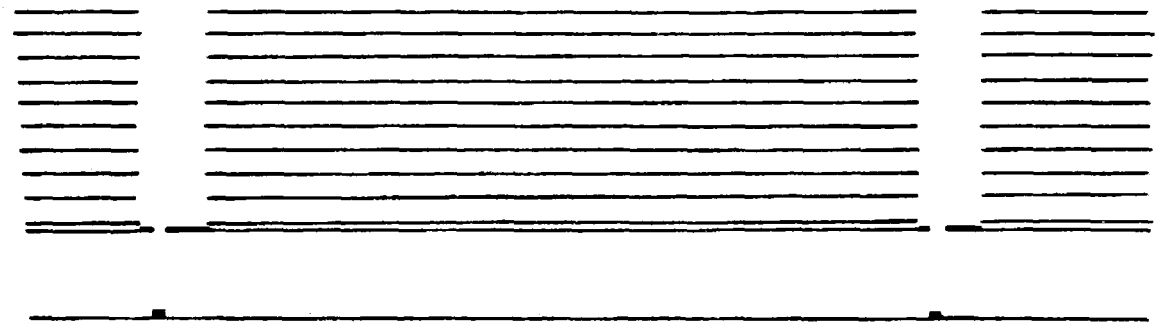
10. Connect the oscilloscope external sync input to the V drive source. Set oscilloscope sweep rate to 2 msec per division. Compare oscilloscope display to figure 6-21b.

11. Connect the video output connector to the monitor input to display the gray scale pattern. A clear, well defined gray scale pattern with all lines straight should be obtained, depending on the quality of the display device.

12. Performance verification of the gray scale function is now complete.



a. Horizontal Rate



b. Vertical Rate

Figure 6-21. Oscilloscope Display of the GRAY SCALE Signal Waveform

NOTE

The gray scale signal is composed of ten levels of brightness, including black and white. Therefore the traditional "ten step" scale actually is composed of nine risers, and eight shades of gray between the extremes. Existing standards and common practice call for a linear gray scale test signal (one with all steps of equal amplitude). The signal provides a nominal 50% APL (Average Picture Level), representative of "typical" television scenes.

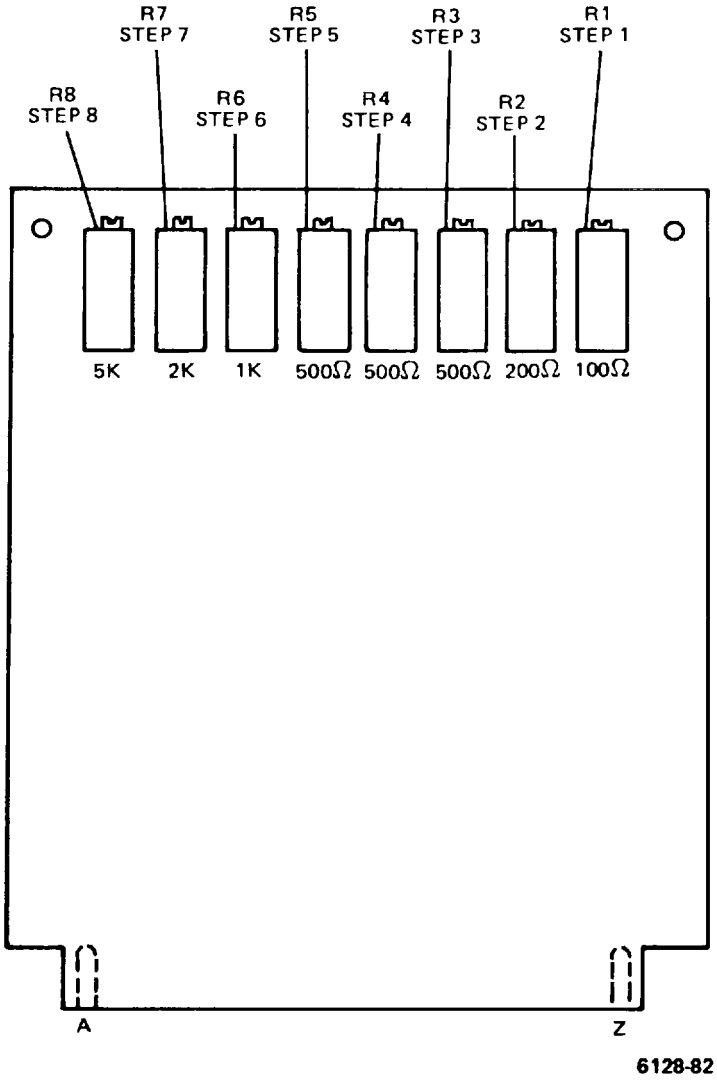


Figure 6-22. Gray Scale Circuit Card Adjustments

6-43. Resolution Adjustment. This function includes many operating conditions and modes, each of which must be adjusted independently. The most common basis for adjustment of signal repetition rate is resolution in tv lines, as detailed in table 6-4. Adjustment can be based on other standards, such as burst frequency, or on other customer specified conditions. The control panel markings are 1 through 10 without reference to units, therefore, allowing various adjustment bases. Adjustments will be set for 100 through 1000 tv lines resolution repetition rate, per table 6-4 for circuit cards 1 through 10, respectively. This function involves the following circuit cards (see figure FO-21):

Multiburst..... Position 19C
Multiburst Clock..... Position 18C
Resolution 1 - Group 4A1..... Position 17C
Resolution 2 - Group 4k2 ..... Position 16C
Resolution 3 - Group 4A3..... Position 15C
Resolution 4 - Group 4A4..... Position 14C
Resolution 5 - Group 4A5..... Position 13C
Resolution 6 - Group 4B6..... Position 12C
Resolution 7 - Group 4B7..... Position 11C
Resolution 8 - Group 4B8..... Position 10C
Resolution 9 - Group 4B9..... Position9C
Resolution 10 - Group 4B10..... Position8C

The group designation identifies components whose values are selected for the particular application.

1. Set the function selector switch at RESOLUTION and resolution selector on REFERENCE.

2. Set the oscilloscope channel 1 input amplitude sensitivity at 0.5v per division. Connect the oscilloscope external sync connector to the H drive source. Set oscilloscope sweep rate to 10 usec per division.

3. The display should appear similar to figure 6-23a, showing approximately 12 cycles of black/white pattern across the horizontal line. The waveform should be square without ringing or overshoot.

4. The repetition rate is adjusted by control R30 located on the MULTIBURST card, figure 6-24.

CAUTION

Measurement technique regarding ringing and overshoot is critical on the fast rise resolution signal. The case of the instrument under test should be firmly grounded to the cases of all other instruments being used. Attention should be paid to coaxial cable grounds to view the optimum output signal from the instrument. The oscilloscope risetime capability must be verified before the output of the instrument may be fully evaluated.

Table 6-4. Resolution Timing (4x3 Aspect Ratio)

Resolution - TV Lines - Actual, H Line	100 133	200 266	300 399	400 533	500 666	600 799	700 933	800 1066	900 1199	1000 1333	
Scan Rate (lines)	Active H Line (usec)			Time	Per	Cycle	(Line Pair)			(msec)	
675/60	42.4	638	319	213	159	127	106	91	80	71	64

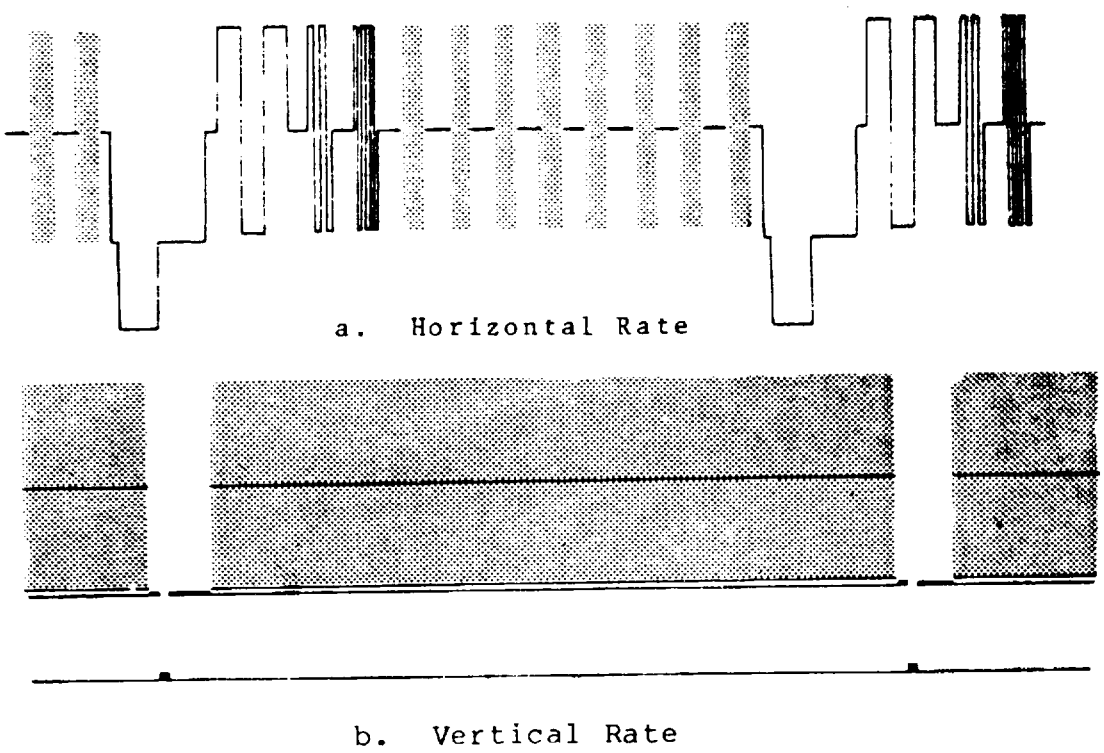


Figure 6-23. Oscilloscope Display of a Typical RESOLUTION Multiburst Signal Waveform

NOTE

By common practice and standards definition, television resolution is the ability of the system to produce an alternate black and white line structure. Each line, black or white, is counted (as opposed to the common "line-pair" terminology of photography). Specifications of tv lines are related to the vertical dimension of the aspect ratio (ratio of horizontal size to vertical size).

The test pattern for resolution is generated electronically as a square wave, providing alternate black and white images in the display. Generally, the bursts are calibrated in 100 line increments, in ascending order, as shown in figure 6-23. Alternate adjustments provide bursts of resolution at any one selected resolution rate, or a continuous presentation of the desired rate over the entire active raster as shown in figure 6-25.

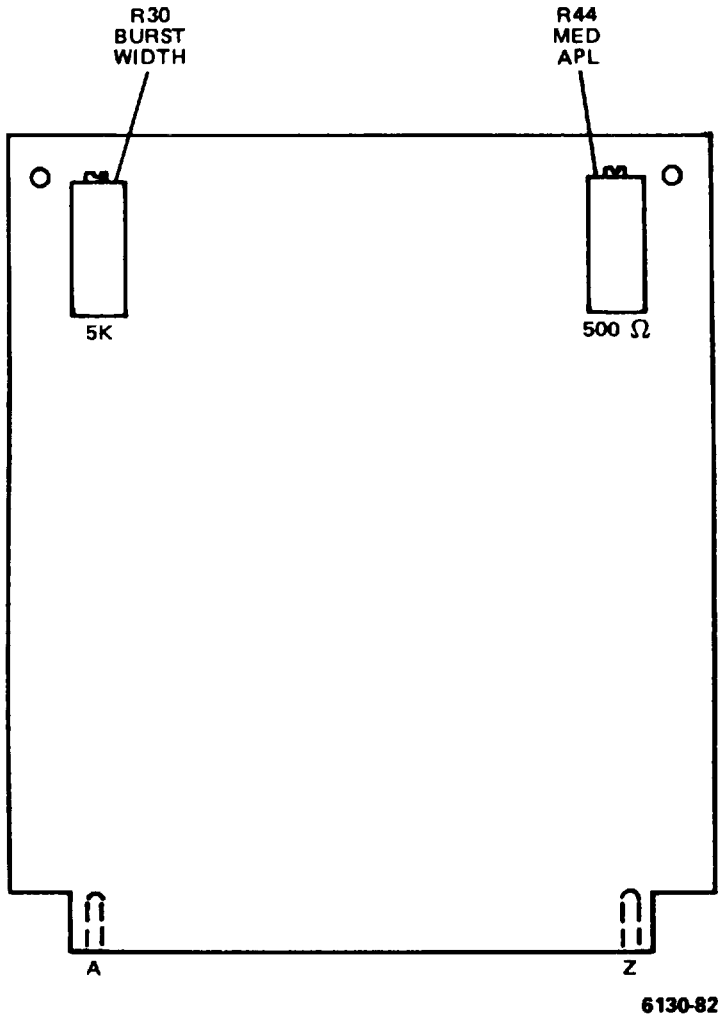


Figure 6-24. Multiburst Circuit Card Adjustments

5. Select RESOLUTION 1 at the front panel. Compare oscilloscope display to figure 6-25a. In this case, there should be approximately 133 cycles of black/white pattern as adjusted for the usual 100 tv lines at 4:3 display ratio. Normally, the burst sequence is adjusted to be 100 tv lines for burst 1,200 tv lines for burst 2, up to 1000 tv lines for burst 10.

6. Set oscilloscope on delayed sweep (0.1 usec per division sweep time), placing the delayed portion of the sweep on the horizontal line to observe the detail of the resolution waveform. The signal should have approximately 10 nsec rise and fall times with a minimum of overshoot and/or ringing.

7. Adjust the control R1 on the RESOLUTION 1 circuit card (figure 6-26) for content as outlined in table 6-4 (638 nsec at the 675-line scan rate).

8. Using control R43 on the RESOLUTION card, adjust the burst cycle to be symmetrical (50% duty cycle, equal length of white and black areas). Readjustment of content as outlined in step 5 may be necessary as duty cycle is balanced.

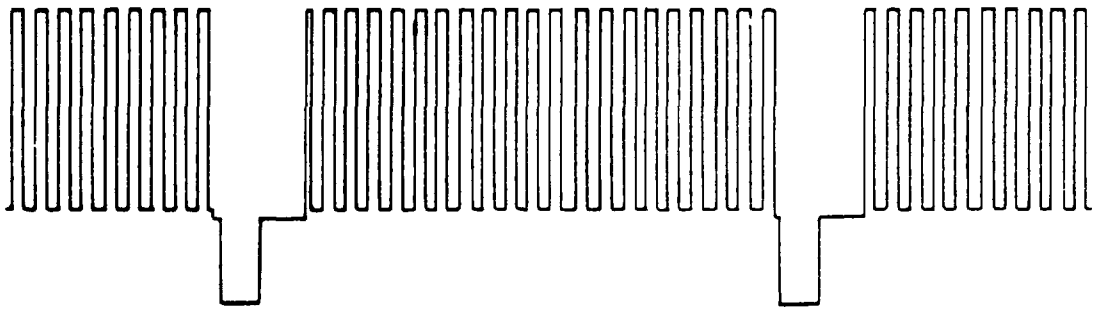
9. Select each resolution rate in turn, adjusting the control R1 on the appropriate RESOLUTION card to obtain the resolution density set forth in table 6-4. Select BURST mode in turn for each resolution rate, comparing oscilloscope display to figure 6-25b. Adjust control R44 of MULTIBURST card to place gray level between burst at 50% of maximum white level. If the video is adjusted from 0 to 1.0v, the gray level should be at 0.5v. Use delayed or undelayed sweep as convenient.

10. Select MULTIBURST mode at the front panel. Set oscilloscope sweep to undelayed. Connect the oscilloscope external sync input to the H drive source. Compare oscilloscope display to figure 6-23a. The waveform should show bursts of resolution separated by gray level in BURSTS mode, or a pattern whith no separation between bursts in the CONTINUOUS mode.

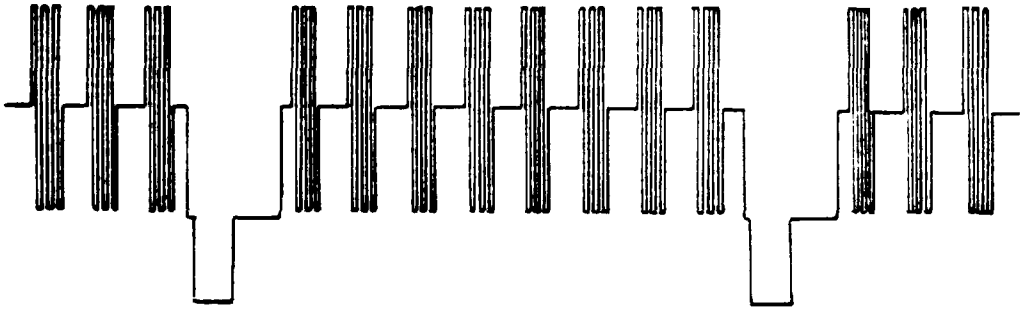
11. Adjust the burst width control R30 located on the MULTIBURST card (figure 6-24) to cover the horizontal line with the resolution pattern as desired. This control was adjusted in step 4, and determines the repetition of the reference pattern as well as location of bursts in other resolution patterns.

12. Connect the video G output connector to the monitor input to display the resolution patterns. Check that all bursts are stable and in straight vertical columns. A clear, well defined resolution pattern should be obtained at each control setting, depending on the quality of the display device.

13. Performance verification of the resolution function is now complete.



a. Typical RESOLUTION Signal, Continuous Mode



b. Typical RESOLUTION Signal, Burst Mode

Figure 6-25. Oscilloscope Display of a Typical RESOLUTION Signal, in CONTINUOUS or BURST, Horizontal Rate

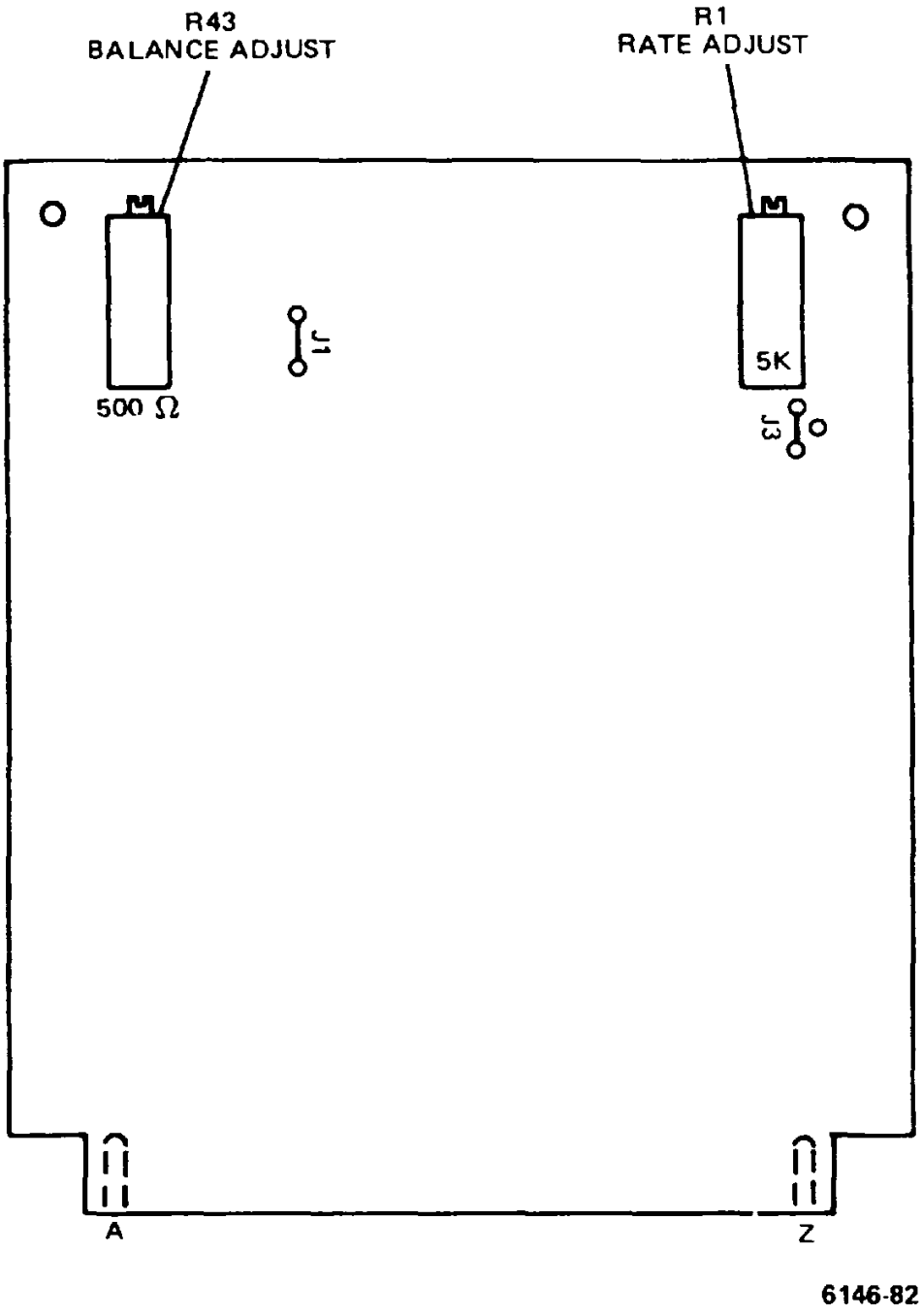


Figure 6-26. Resolution Circuit Card Adjustments

Section VI. WIRE LISTS

6-44. Introduction. This section contains wire lists for the Test Pattern Generator. The wire lists, tables 6-5 through 6-21, contain interconnecting wiring data between circuit board assembly and the front panel (figure 6-1) and rear panel assemblies (figure 6-2). The wire list entries are explained in paragraph 6-45. All card locations are shown in figures FO-20 and FO-21.

6-45. Wire List Column Identification. Entries for each column of the wire lists are explained as follows:

a. CONNECTOR PIN NUMBER. Indicates the circuit board connector pin number.

b. FUNCTION. Name of signal voltage.

c. DESTINATION. Terminating point of the respective wire run.

Table 6-5. V Bar Wiring Interconnections

Connector Pin	Function	Destination
Z	--	
Y	--	
X	Width In	Control Panel, R1, H Spacing
W	Ground	V Bar, Pin N; Ground Buss
V	+5v	V Bar, Pin S, Pin C; Control Panel, S1, Function Select
U	Position Control In	Control Panel, R3, H Position
T	-H Gate In	H Bar, Pin X; H Window, Pin T; V Window, Pin P; Pulse Input, Pin P
S	V Bar On	V Bar, Pin V, Pin C; Control Panel, S1, Function Select
R	-5v	5v Buss; Power Regulator, Fin V
P	--	
N	Ground	V Bar, Pin W; Ground Buss
M	--	
L	Bar Select	Control Panel, S1, Function Select
K	-V Gate	V Window, Pin S; Pulse Input, Pin T
J	-V Input	H Bar, Pin N
H	Output	H Window, Pin L; V Window, Pin L; Gray Scale, Pin B; Polarity, Pin Y
F	Gated V In	H Bar, Pin M
E	V Bar Size In	V Bar, Pin D
D	Width Out	V Bar, Pin E
C	Width In	V Bar, Pin S, Pin V; Control Panel, S1, Function Select
B	--	
A	--	
	Ground	Control Panel, R5, Video Level; Power Regulator,

Table 6-6. H Bar Wiring Interconnections

Connector Pin	Function	Destination
Z	--	
Y	--	
X	-H Gate Input	H Window, Pin T; V Bar, Pin T; V Window, Pin P; Pulse Input, Pin P
W	Dot Select Input	Control Panel, S1, Function Select
V	H Bar On	H Bar, Pin F; Control Panel, S1, Function Select
U	+V Gate Input	V Window, Pin W; Pulse Input, Pin U
T	--	
S	-5v	-5v Buss; Power Regulator, Pin V
R	V Trigger Output	H Bar, Pin E
P	--	
N	V Output	V Bar, Pin J
M	Signal Out	V Bar, Pin F
L	Ground	Ground Buss
K	--	
J	-5v	5v Buss; Power Regulator, Pin V
H	--	
F	H Bar On	H Bar, Pin V; Control Panel, S1, Function Select
E	--	
D	Position Input	Control Panel, R4, V Position
C	Width Input	Control Panel, R2, V Spacing
B	--	
A	--	

Table 6-7. H Window Wiring Interconnections

Connector Pin	Function	Destination
Z	H Position Control On (+5v)	H Window, Pins V, E, D, A; Control Panel, S1, Function Select
Y	H Position Control Out	H Window, Pin X
X	H Position Control In	H Window, Pin Y
W	--	
V	+5v	H Window, Pins Z, E, D, A; Control Panel, S1, Function Select
U	-5v	-5v Buss; Power Regulator, Pin V
T	-H Gate Input	H Bar, Pin X; V Bar, Pin T; V Window, Pin P; Pulse Input, Pin P
S	--	
R	--	
P	--	
N	Ground	Ground Buss
M	--	
L	H Window Output	V Bar, Pin H; V Window, Pin L; Gray Scale, Pin B; Polarity, Pin Y
K	--	
J	--	
H	--	
F	-5v	-5v Buss; Power Regulator, Pin V
E	H Window On	H Window, Pins Z, V, D, A; Control Panel, S1, Function Select
D	+5v	H Window, Pins Z, V, E, A; Control Panel, S1, Function Select
C	H Width Control Input	H Window, Pin B

Table 6-7. H Window Wiring Interconnections - Continued

Connector Pin	Function	Destination
B	H Width Control Output	H Window, Pin C
A	H Width Control On	H Window, Pins Z, V, E, D; Control Panel, S1, Function Select

Table 6-8. V Window Wiring Interconnections

Connector Pin	Function	Destination
Z	V Position Out	V Window, Pin X
Y	V Position On (+5v)	V Window, Pins V, K, F, B; Control Panel, S1, Function Select
X	V Position In	V Window, Pin Z
W	+V Gate In	H Bar, Pin U; Pulse Input, Pin U
V	+5v	V Window, Pins Y, K, F, B; Control Panel, S1, Function Select
U	-5v	5v Buss; Power Regulator, Pin V
T	--	
S	-V Gate In	V Bar, Pin K; Pulse Input, Pin T
R	-V Position Out	V Window, Pin D
P	-H Gate Input	H Window, Pin T; H Bar, Pin X; V Bar, Pin T; Pulse Input, Pin P
N	+H Gate Out	V Window, Pin E
M	Ground	Ground Buss
L	V Window Signal Out	H Window, Pin L; V Bar, Pin H; Polarity, Pin Y; Gray Scale, Pin B
K	V Window On (+5v)	V Window, Pins Y, V, F, B; Control Panel, S1, Function Select
J	--	
H	--	
F	+5v	V Window, Pins Y, V, K, B; Control Panel, S1, Function Select
E	+H Gate In	V Window, Pin N
D	-V Position Out	V Window, Pin R
C	V Window In	V Window, Pin A
B	V Window On (+5v)	V Window, Pins Y, V, K, F; Control Panel, S1, Function Select
A	V Window Out	V Window, Pin C

Table 6-9. Gray Scale Control Wiring Interconnections

Connector Pin	Function	Destination
Z	--	
Y	--	
X	+12v	Power Regulator, Pin Y; Heat Sink, Left Side, +12v; Chassis, TB2-3
W	+5v	+5v Buss; Power Regulator, Pin C
V	Gray Scale In	Gray Scale, Pin C, Pin A; Multiburst, Pin Z
U	-5v	-5v Buss; Power Regulator, Pin V
T	Gray Scale Out	Control Panel, R5, Video Level
S	Ground	Gray Scale Control, Pin L; Ground Buss
R	--	
P	+Blanking	Pulse Input, Pin K; Polarity, Pin U; Video, Pin F
N	Clock Output	Gray Scale, Pin N
M	--	
L	Ground	Gray Scale Control, Pin S; Ground Buss
K	-5v	5v Buss; Power Regulator, Pin V
J	--	
H	--	
F	-H Gate Input	Pulse Input, Pin L
E	--	
D	+5v	Gray Scale, Pin Y; Gray Scale Control, Pin B; Control Panel, S1, Function Select
C	Width Control In	Gray Scale Control, Pin A

Table 6-9. Gray Scale Control Wiring Interconnections - Continued

Connector Pin	Function	Destination
B	Width Input	Gray Scale Control, Pin D; Gray Scale Pin Y; Control Panel, S1, Function Select
A	Width Output	Gray Scale Control, Pin C

Table 6-10. Gray Scale Wiring Interconnections

Connector Pin	Function	Destination
Z	Ground	Ground Buss
Y	+5v	Gray Scale Control, Pin D, Pin B; Control Panel, S1, Function Select
X	--	
W	Prime A	Gray Scale, Pin L
V	--	
U	Prime B	Gray Scale, Pin H
T	Bi-stable Trigger Out	Gray Scale, Pin E
S	--	
R	--	
P	+H Gate In	Pulse Input, Pin R
N	Clock In	Gray Scale Control, Pin N
M	--	
L	Prime A Out	Gray Scale, Pin W
K	Ground	Ground Buss
J	--	
H	Prime B Out	Gray Scale, Pin U
F	--	
E	Bi-stable Trigger In	Gray Scale, Pin T
D	-5v	-5v Buss; Power Regulator, Pin V
C	Gray Scale Black In	Gray Scale, Pin A; Gray Scale Control, Pin V; Multiburst, Pin Z
B	Black Video	V Window, Pin L; H Window, Pin L V Bar, Pin H; Polarity, Pin Y
A	Gray Scale In	Gray Scale, Pin C; Gray Scale Control, Pin V; Multiburst, Pin Z

Table 6-11. Pulse Output Wiring Interconnections

Connector Pin	Function	Destination
Z	+12v	Chassis, TB2-3
Y	+20VDC Unreg	Chassis, TB2-2
X	Blank Out	Rear Panel, J6, Blanking
W	H Drive Out	Rear Panel, J2, H Drive
V	V Drive Out	Rear Panel, J4, V Drive
U	Sync Out	Rear Panel, J8, Sync
T	--	
S	Ground	Pulse Output, Pins P, N, M, L Ground Buss
R	-5v	-5v Buss; Chassis, TB2-4
P	Ground	Pulse Output, Pins S, N, M, L; Ground Buss
N	Ground	Pulse Output, Pins S, P, M, L; Ground Buss
M	Ground	Pulse Output, Pins S, P, N, L; Ground Buss
L	Ground	Pulse Output, Pins S, P, N, M; Ground Buss
K	-5v	-5v Buss; Chassis TB2-4
J	--	
H	--	
F	+5v	+5v Buss; Chassis, TB2-1
E	Sync In	Sync, Pin K
D	Blank In	Drive/Blanking, Pin K
C	V Drive In	Drive/Blanking, Pin H
B	H Drive In	Drive/Blanking, Pin E
A	--	

Table 6-12. Sync Wiring Interconnections

Connector Pin	Function	Destination
Z	Count 4 Input	Sync Count, Pin D
Y	Count 2 Input	Sync Count, Pin C
X	Count 1 Input	Sync Count, Pin B
W	Count 8 Input	Sync Count, Pin E
V	V Trigger Input	Drive/Blanking, Pin B
U	H Front Porch Control	Sync, Pins T, N, M, H; Ground Buss
T	Serration Control	Sync, Pins U, N, M, H; Ground Buss
S	--	
R	--	
P	--	
N	Military Control	Sync, Pins U, T, M, H; Ground Buss
M	Equalizing Control	Sync, Pins U, T, N, H; Ground Buss
L	-5v	-5v Buss; Chassis, TB2-4
K	Sync Output	Pulse Output, Pin E
J	+H Input	Sync Count, Pin T
H	Ground	Sync, Pins N, M, T, U; Ground Buss
F	2H Input	Drive/Blanking, Pin S
E	--	
D	+2H Front Porch Delay Out	Sync Count, Pin R Delay Out
C	+5v	+5v Buss; Chassis, TB2-1
B	--	
A	--	

Table 6-13. Drive/Blanking Wiring Interconnections

Connector Pin	Function	Destination
Z	+5v	+5v Buss; Chassis, TB2-1
Y	Ground	Drive/Blanking, Pin U; Ground Buss
X	--	
W	--	
V	Crystal On	+5v Buss; Chassis, TB2-1
U	AFC Input	Drive/Blanking, Pin Y; Ground Buss
T	--	
S	2H Master Oscillator Output	Sync, Pin F
R	-Reset Input	Sync Count, Pin Y
P	--	
N	-5v	5v Buss; Chassis, TB2-4
M	--	
L	--	
K	+Blanking Output	Pulse Output, Pin D
J	--	
H	+V Drive Output	Pulse Output, Pin C
F	--	
E	+H Drive Output	Pulse Output, Pin B
D	V Blank Width Input	Sync Count, Pin W
C	V Drive Width Input	Sync Count, Pin X
B	-V Trigger Output	Sync, Pin V
A	-H Input	Sync Count, Pin U

Table 6-14. Sync Count Wiring Interconnections

Connector Pin	Function	Destination
Z	+5v	+5v Buss; Chassis, TB2-1
Y	Reset Out	Drive/Blanking, Pin R
X	V Drive Width Output	Drive/Blanking, Pin C
W	V Blank Width Output	Drive/Blanking, Pin D
V	Ground	Ground Buss
U	-H Output	Drive/Blanking, Pin A
T	+H Output	Sync, Pin J
S	--	
R	2H Input	Sync, Pin D
N	--	
L	--	
K	--	
J	--	
H	--	
F	--	
E	Count 8 Out	Sync, Pin W
D	Count 4 Out	Sync, Pin Z
C	Count 2 Out	Sync, Pin Y
B	Count 1 Out	Sync, Pin X
A	--	

Table 6-15. Power Regulator Wiring Interconnections

Connector Pin	Function	Destination
Z	+5v Ref	Heat Sink, Right Side, +5v Ref
Y	+12v	+12v Buss; Chassis, TB2-3; Heat Sink, Left Side, +12v
X	--	
W	--	
V	-4.3v	5v Buss; Heat Sink, Left Side, -4.3v
U	--	
T	Ground	Ground Buss
S	--	
R	--	
N	--	
M	--	
L	--	
K	AC In	Chassis, TB1-5
J	DC (12v) Out	Chassis, TB2-2; Heat Sink, Left Side, +E
H	AC In	Chassis, TB1-7
F	--	
E	--	
D	--	
C	+5v Reg	+5v Buss; Control Panel, S1, Function Select; Heat Sink, Right Side, +5v; Chassis, TB2-1
B	T-1 Center Tap	Chassis, TB1-6; Ground Buss; Heat Sink, Center

Table 6-15. Power Regulator Wiring Interconnections - Continued

Connector Pin	Function	Destination
A	-5v	Pulse Input, Pin W; Polarity, Pin W; Video, Pin U, Pin L; Resolution Pin U, Pin J; Multiburst Clock, Pin E; Multiburst, Pin S; Heat Sink, Left Side, -5v; Chassis, TB2-4
	Ground	Rear Panel, J8, Ground; Heat Sink, Left Side, Ground; V Bar, Ground

Table 6-16. Pulse Input Wiring Interconnections

Connector Pin	Function	Destination
Z	H Drive Input	Control Panel, TP1, H Drive
Y	V Drive Input	Control Panel, TP2, V Drive
X	--	
W	-5v	Power Regulator, Pin A; Polarity, Pin W; Video, Pin U, Pin L; Resolution, Pin U, Pin J; Multiburst Clock, Pin E; Multiburst, Pin S; Heat Sink, Left Side, -5v; Chassis, TB2-4
V	--	
U	+V Gate Output	H Bar, Pin U; V Window, Pin W
T	-V Gate Output	V Window, Pin S; V Bar, Pin K
S	--	
R	+H Gate Output	Gray Scale, Pin P
P	-H Gate Output	V Bar, Pin T; H Bar, Pin X; H Window, Pin T; V Window, Pin P
N	Ground	Ground Buss
L	-Blanking Output	Gray Scale Control, Pin F
K	+Blanking Output	Polarity, Pin U; Video, Pin F; Gray Scale Control, Pin P; Multiburst, Pin J
J	--	
H	--	
F	+Sync Output	Video, Pin A
E	--	
D	+5v	+5v Buss; Power Regulator, Pin C; Control Panel, S1, Function Select
C	--	

Table 6-16. Pulse Input Wiring Interconnections - Continued

Connector Pin	Function	Destination
B	Sync Input	Control Panel, TP4, Sync
A	Blanking Input	Control Panel, TP3, Blanking

Table 6-17. Polarity Wiring Interconnections

Connector Pin	Function	Destination
Z	--	
Y	Polarity In	V Bar, Pin H; H Window, Pin L; V Window, Pin L; Gray Scale, Pin B
X	--	
W	-5v	Power Regulator, Pin A; Video, Pin U, Pin L; Pulse Input, Pin W; Resolution, Pin U, Pin J; Multiburst Clock, Pin E; Multiburst, Pin S; Chassis, TB2-4, Heat Sink, Left Side, -5v
V	+5v	+5v Buss; Power Regulator, Pin C
U	+Blank In	Pulse Input, Pin K; Video, Pin F; Multiburst, Pin J; Gray Scale Control, Pin P
T	Pattern Out	Video, Pin S
S	--	
R	--	
P	Pattern In	Polarity, Pin B; Multiburst, Pin T
N	Ground	Ground Buss
M	--	
L	White On	Control Panel, S3, Pattern Polarity
K	--	
J	Flat Field On	Control Panel, S1, Function Select
H	--	
F	--	
E	--	
D	--	
C	Black On	Control Panel, S3, Pattern Polarity
B	Polarity Out	Polarity, Pin P; Multiburst, Pin T
A	--	

Table 6-18. Video Wiring Interconnections

Connector Pin	Function	Destination
Z	+5v	+5v Buss; Power Regulator, Pin C
Y	--	
X	Ground	Video, Pins V, R, E, D, B; Ground Buss; Resolution, Pins C, E, H, K, L
W	Resolution In	Resolution, Pin D
V	Ground	Video, Pins X, R, E, D, B; Ground Buss; Resolution, Pins C, E, H, K, L
U	5v	Power Regulator, Pin A; Video, Pin L; Polarity, Pin W; Pulse Input, Resolution, Pins U, J; Multiburst Clock, Pin E; Multiburst, Pin S; Chassis, TB2-4; Heat Sink, Left Side, -5v
T	--	
S	Invert Pattern In	Polarity, Pin T
R	Ground	Video, Pins V, X, E, D, B; Ground Buss; Resolution, Pins C, E, H, K, L
P	Level In	Control Panel, R5, Video Level
N	--	
M	--	
L	-5v	Power Regulator, Pin A; Video, Pin U; Polarity, Pin W; Pulse Input, in W; Resolution, Pins U, J; Multiburst Clock, Pin E; Multiburst, in S; Chassis, TB2-4; Heat Sink, Left Side, -5v
K	+5v	+5v Buss; Power Regulator, Pin C
J	--	
H	--	
F	+Blanking In	Polarity, Pin U; Pulse Input, Pin K; Multiburst, Pin J; Gray Scale Control, Pin P

Table 6-18. Video Wiring Interconnections - Continued

Connector Pin	Function	Destination
E	Blank On	Video Pins D, B, R, V, X; Ground Buss; Resolution, Pins C, E, H, K, L
D	Sync On	Video, Pins E, B, R, V, X; Ground Buss; Resolution, Pins C, E, H, K, L
C	Video Out	Control Panel, TP5, Video G
B	Ground	Video, Pins D, E, R, V, X; Ground Buss; Resolution, Pins C, E, H, K, L
A	+Sync In	Pulse Input, Pin F

Table 6-19. Resolution Wiring Interconnections

Connector Pin	Function	Destination
Z	--	
Y	--	
X	--	
W	--	
V	--	
U	-5v	Resolution, Pin J; Multiburst Clock, Pin E; Multiburst, Pin S; Polarity, Pin W; Pulse Input, Pin W; Power Regulator, Pin A; Chassis, TB2-4; Heat Sink, Left Side, -5v
T	--	
S	--	
R	Multiburst Control	Multiburst, Pin F
P	Control	Resolution 1-Multiburst Clock, Pin B Resolution 2-Multiburst Clock, Pin M Resolution 3-Multiburst Clock, Pin A Resolution 4-Multiburst Clock, Pin N Resolution 5-Multiburst Clock, Pin Z Resolution 6-Multiburst Clock, Pin P Resolution 7-Multiburst Clock, Pin Y Resolution 8-Multiburst Clock, Pin R Resolution 9-Multiburst Clock, Pin X Resolution 10-Multiburst Clock, Pin S
N	Select	Control Panel, S2, Resolution Mode
M	Multiburst On	Multiburst Clock, Pin T; Multiburst, Pin R; Control Panel, S2, Resolution Mode
L	Ground	Resolution, Pins K, H, E, C; Ground Buss; Video, Pins X, V, R, E, D, B
K	Ground	Resolution, Pins L, H, E, C; Ground Buss; Video, Pins X, V, R, E, D, B

Table 6-19. Resolution Wiring Interconnections - Continued

Connector Pin	Function	Destination
J	-5v	Power Regulator, Pin A; Pulse Input, Pin W; Multiburst Clock, Pin E; Multiburst, Pin S; Resolution, Pin U; Polarity, Pin W; Heat Sink, Left Side, -5v; Chassis, TB2-4
H	Ground	Resolution, Pins L, K, E, C; Ground Buss; Video, Pins X, V, R, E, D, B
F	--	
E	Ground	Resolution, Pins L, K, H, C; Ground Buss; Video, Pins X, V, R, E, D, B
D	Resolution Output	Video, Pin W
C	Ground	Resolution, Pins L, K, H, E; Ground Buss; Video, Pins X, V, R, E, D, B
B	Resolution On (+5v)	+5v Buss; Power Regulator, Pin C
A	Resolution On (+5v)	Multiburst, Pin D; Control Panel, S1, Function Select

Table 6-20. Multiburst Clock Wiring Interconnections

Connector Pin	Function	Destination
Z	Burst 5	Resolution (5), Pin P
Y	Burst 7	Resolution (7), Pin P
X	Burst 9	Resolution (9), Pin P
W	Stop Pulse A	Multiburst, Pin W, Pin E
V	--	
U	Ground	Ground Buss
T	Multiburst On (+5v)	Multiburst, Pin R; Resolution, Pin M; Control Panel, S2, Resolution Mode
S	Burst 10	Resolution (10), Pin P
R	Burst 8	Resolution (8), Pin P
P	Burst 6	Resolution (6), Pin P
N	Burst 4	Resolution (4), Pin P
M	Burst 2	Resolution (2), Pin P
L	-Ref Pulse	Multiburst, Pin N
K	Ref On (+5v)	Control Panel, S2, Resolution Mode
J	Clock In	Multiburst, Pin M
H	-H Gate In	Pulse Input, Pin L; Gray Scale Control, Pin F
F	--	
E	-5v	Power Regulator, Pin A; Resolution, Pin U, Pin J; Multiburst, Pin S; Polarity, Pin W; Pulse Input, Pin W; Chassis, TB2-4; Heat Sink, Left Side, -5v
D	--	
C	+Ref Pulse	Multiburst, Pin L
B	Burst 1	Resolution (1), Pin P
A	Burst 3	Resolution (3), Pin P

Table 6-21. Multiburst Wiring Interconnections

Connector Pin	Function	Destination
Z	Gray Scale Signal In	Gray Scale Control, Pin V; Gray In Scale, Pin C, Pin A
Y	Med APL On Multiburst	Multiburst, Pin C, Pin A; Control Panel, S4, Resolution Format
X	Cont On	Control Panel, S4, Resolution Format
W	Pulse In	Multiburst, Pin E; Multiburst Clock, Pin W
V	Bar On	Multiburst, Pin P; Control Panel, S2, Resolution Mode
U	--	
T	Signal Out	Polarity, Pin B, Pin P
S	-5v	Power Regulator, Pin A; Multiburst Clock, Pin E; Resolution, Pin U, Pin J; Polarity, Pin W; Pulse Input, Pin W; Chassis, TB2; Heat Sink, Left Side, -5v
R	Multiburst On (+5v)	Multiburst Clock, Pin T; Resolution, Pin M; Control Panel, S2, Resolution Mode
P	Ref On	Multiburst, Pin V; Control Panel, S2, Resolution Mode
N	Ref In	Multiburst Clock, Pin L
M	Clock Out	Multiburst Clock, Pin J
L	+Ref Pulse In	Multiburst Clock, Pin C
K	Ground	Ground Buss
J	+H Gate In	Video, Pin F; Polarity, Pin U; Pulse Input, Pin K; Gray Scale Control, Pin P
H	Width Control In	Multiburst, Pin B
F	Multiburst Control	Resolution, Pin R

Table 6-21. Multiburst Wiring Interconnections - Continued

Connector Pin	Function	Destination
E	Stop Pulse In	Multiburst, Pin W; Multiburst Clock, Pin W
D	Resolution On (+5v)	Resolution, Pin A; Control Panel, S1, Function Select
C	Burst On	Multiburst, Pin A, Pin Y; Control Panel, S4, Resolution Format
B	Width Control Out	Multiburst, Pin H
A	Width Control On	Multiburst, Pin C, Pin Y; Control Panel, S4, Resolution Format

APPENDIX A

REFERENCES

DA Pam 310-1	Consolidated Index of Army Publications and Blank Forms.
SB 11-573	Painting and Preservation Supplies Available for Field Use for Electronics Command Equipment.
TM 746-10	Field Instructions for Painting and Preserving Electronics Command Equipment.
TM 740-90-1	Administrative Storage of Equipment.
TM 38-750	The Army Maintenance Management System (TAMMS).
TM 11-6625-3025-24P EE426-AA-PLL-010/E154 VII210 T.O. 33A1-8-902-4-1	Repair Parts and Special Tools (RPSTL): Generator, Test Pattern SG-1223/T (NSN 6625-01-127-6846)
TM 750-244-2	Procedure for Destruction of Electronics Materiel to Prevent Enemy Use. (Electronics Command.)
TM 11-6625-2953-14	Operator's, Organizational, Direct Support, and General Support Maintenance Manual for Multimeter AN/USM-451 (NSN 6625-01-060-6804)
TM 11-6625-2735-14 0969-LP-170-1090 T.O. 33A1-13-498-1	Operator's, Organizational, Direct Support, and General Support Maintenance Manual (Including Depot Maintenance) for Oscilloscope OS-261/U (NSN 6625-00-127-0079)

APPENDIX B

MAINTENANCE ALLOCATION

Section I. INTRODUCTION

B-1. General. This appendix provides a summary of the maintenance operations for the Generator Test Pattern SG 1223/T It authorizes categories of maintenance for specific maintenance functions on repairable items and components and the tools and equipment required to perform each function.

B-2. Maintenance Concept. Three levels of maintenance shall be utilized for the equipment as follows:

Organizational Level
General Support Level
Depot Level.

a. Organization Maintenance. That maintenance which is the responsibility of and performed by a using organization on its assigned equipment. Its phases normally consist of inspecting, servicing, lubricating, and adjusting, and the replacement of parts, minor assemblies and subassemblies. This level is designated by an O in the Maintenance Category columns in Section II.

b. General Support Maintenance. That maintenance which is the responsibility of and performed by designated maintenance activities to support lower level activities. General Support Maintenance is normally accomplished in fixed shops. This level is designated by an H in the Maintenance Category columns in Section II.

c. Depot Maintenance. That maintenance which is the responsibility of and performed by designated maintenance activities, to augment stocks of serviceable material, and to support lower level activities by the use of more extensive shop facilities, equipment and personnel of higher technical skills than are available at the lower level of maintenance. Its phases normally consist of inspection, test, repair, modification, alteration, modernization, conversion, overhaul reclamation or rebuild of parts, assemblies, subassemblies, components, equipment end items, and weapon systems; and the manufacture of critical non-available parts. Depot Maintenance is normally accomplished in fixed shops. This level is designated by a D in the Maintenance Category columns in Section II.

B-3. Maintenance Function. Maintenance functions for the Generator, Test Pattern SG 1223 T are defined as follows:

a. Inspect. To determine the serviceability of an item by comparing its physical, mechanical, and/or electrical characteristics with established standards through examination.

b. Test. To verify serviceability and to detect incipient failure by measuring the mechanical or electrical characteristics of an item and comparing those characteristics with prescribed standards.

c *Service.* Operations required periodically to keep an item in proper operating condition, i.e., to clean (decontaminate), to preserve, to drain, to paint, or to replenish fuel, lubricants, hydraulic fluids, or compressed air supplies.

d Adjust. To maintain, within prescribed limits, by bringing into proper or exact position, or by setting the operating characteristics to the specified parameters.

e. Align. To adjust specified variable elements of an item to bring about optimum or desired performance.

f. Calibrate. To determine and cause corrections to be made or to be adjusted on instruments or test measuring and diagnostic equipments used in precision measurement. Consists of comparisons of two instruments, one of which is a certified standard of known accuracy, to detect and adjust any discrepancy in the accuracy of the instrument being compared.

g Install. The act of emplacing, seating, or fixing into position an item, part, or module (component or assembly) in a manner to allow the proper functioning of the equipment or system.

h. Replace. The act of substituting a serviceable like type part, subassembly, or module (component or assembly) for an unserviceable counterpart.

i. Repair. The application of maintenance service (inspect, test, service, adjust, align, calibrate, or replace) or other maintenance actions (welding, grinding, riveting, straightening, facing, remachining, or resurfacing) to restore serviceability to an item by correcting specific damage, fault, malfunction, or failure in a part, subassembly, module (component or assembly), end item, or system.

j. Overhaul. That maintenance effort (service/ action) necessary to restore an item to a completely serviceable/operational condition as prescribed by maintenance standards (i.e., DMWR) in appropriate technical publications. Overhaul is normally the

highest degree of maintenance performed by the Army. Overhaul does not normally return an item to like new condition.

k. Rebuild. Consists of those services/actions necessary for- the restoration of unserviceable equipment to a like new condition in accordance with original manufacturing standards. Rebuild is the highest degree of materiel maintenance applied to Army equipment. The rebuild operation includes the act of returning to zero those age measurements (hours, miles, etc.) considered in classifying Army equipments/components.

B-4. Column Entries.

a. Column 1, Group Number-. Column 1 lists group numbers, the purpose of which is to identify components, assemblies, subassemblies, and modules pith the next higher assembly.

b. Column 2, Component/Assembly). Column 2 contains the noun names of components, assemblies, subassemblies, and modules for which maintenance is authorized.

*c. Column. 3, .*Ma*inten*ance *Function.* Column 3 the functions to be performed on the item listed in Column 2. When items are listed without maintenance functions, it is solely) for the purpose of having the group numbers in the MAC and RPSTL, coincide.

d. Column 4,Maintenance Category . Column 4 specifies by the listing of a worktime figure in the appropriate subcolumn(s), the lowest level of maintenance authorized to perform the function listed in Column 3. This figure represents the active time required to perform that maintenance function at the indicated category of maintenance. If the number or complexity of the tasks within the listed maintenance function vary at different maintenance categories, appropriate worktime figures will be shown for each category. The number of task-hours specified by the worktime figure represents the average time required to restore an item (assembly, subassembly, component module, end item or system) to a serviceable condition under typical field operating conditions. This time includes preparation time, troubleshooting time, and quality assurance/quality control time in addition to the time required to perform the specific tasks identified for the maintenance functions authorized in the maintenance allocation chart. Subcolumns of Column 4 are as follows:

C Operator/Crew
O Organizational
F Direct Support
H General Support
D Depot.

e. Column 5, Tools and Equipment. Column 5 specifies, by code, those common tool sets (not individual tools), and special tools, test, and support equipment required to perform the designated function.

f. Column 6, Remarks. Column 6 contains an alphabetic code which leads to the remark in Section IV, Remarks, which is pertinent to the item opposite the particular code.

B-5. Tool and Test Equipment Requirements (Section III).

a. Tool or Test Equipment Reference Code. The numbers in this column coincide with the numbers used in the tools and equipment column of the MAC. The numbers indicate the applicable tool or test equipment for the maintenance functions.

b. Maintenance Category. The codes in this column indicate the maintenance category allocated the tool or test equipment.

c. Nomenclature. This column lists the noun name and nomenclature of the tools and test equipment required to perform the maintenance functions.

d. National/NA TO Stock Number. This column lists the National/NATO stock number of the specific tool or test equipment.

e. Tool Number. This column lists the manufacturer's part number of the tool followed by the Federal Supply Code for manufacturers (5-digit) in parentheses.

B-6. Remarks (Section IV).

a. Reference Code. This code refers to the appropriate item in Section II, Column 6.

b. Remarks. This column provides the required explanatory information necessary to clarify items appearing in Section II.

SECTION II. MAINTENANCE ALLOCATION CHART FOR TEST PATTERN GENERATOR SG-1223/T

(1) GROUP NUMBER	(2) COMPONENT ASSEMBLY	(3) MAINTENANCE FUNCTION	(4) MAINTENANCE CATEGORY C	O	F	H	D	(5) TOOLS AND EQUIPMENT	(6) REMARKS
00	GENERATOR, TEST PATTERN	INSPECT		0.1					A
		SERVICE		0.2				4	B
		REPLACE		0.1					
		REPAIR		0.1				1,4	C
		TEST				1.0		2,3,4	F
		OVERHAUL					60.0	1,2,3, 4,5	
		REBUILD					80.0	1,2,3, 4,5	
01	TEST PATTERN GENERATOR	ADJUST				0.2		1,2,3, 4	
		REPLACE				0.1		4	
		REPAIR				1.5		1,2,4,5	
		REPAIR				1.5		6	
0101	PRINTED CIRCUIT CARDS L-2003,L-2004,L-2008, L-2009,L-2011,L-2012, L-2013,L-2014,L-2015, L-2016,L-2020,L-2024, L-2025,L-2028,L-2029, L-2110,L-2117	ADJUST				0.2		1,2,3, 4	D
		REPLACE				0.2		4	
		REPAIR					1.5	6	
0102	CARD NEST ASSEMBLIES B, C	REPAIR				1.5		1,2,4,5	
0103	FRONT PANEL ASSEMBLY	REPAIR				1.5		1,2,4	E

SECTION III. TOOL AND TEST EQUIPMENT REQUIREMENTS FOR TEST PATTERN GENERATOR SG-1223/T

Tool or Test Equipment Ref Code	Maintenance Category	Nomenclature	National/NATO Stock Number	Tool Number
1	O,H,D	DIGITAL MULTIMETER, AN USM 451	6625-00-168-0585	
2	H,D	OSCILLOSCOPE OS-261/U	6625-00-127-0079	
3	H,D	ACCESSORIES KIT, IL		
4	O,H,D	TOOL KIT, TK-105/G	5180-00-610-8177	
5	H,D	TOOL KIT, WIRE WRAP, ELECTRICAL CONNECTOR		
6	D	PC CARD REPAIR TOOL KIT	3439-00-196-0703	

SECTION IV. REMARKS FOR TEST PATTERN GENERATOR SG-1223/T

Reference Code	Remarks
A	VISUAL EXTERNAL
B	REMOVE DUST FROM INTERNAL ASSEMBLIES
C	ORGANIZATIONAL REPAIR IS LIMITED TO FUSE REPLACEMENT
D	APPROPRIATE ADJUSTMENTS PERFORMED AFTER REPLACEMENT OF THE FOLLOWING CARDS: L-2003, L-2004, L-2008, L-2011, L-2013, L-2014, L-2015, L-2020, L-2024, L-2028, L-2029, L-2110, OR L-2117
E	REPAIR CONSISTS OF FRONT PANEL OR CHASSIS COMPONENT REPLACEMENT
F	EXECUTION OF PERFORMANCE TEST MAY REQUIRE CONCURRENT ADJUSTMENTS

APPENDIX C

COMPONENTS OF END ITEM LIST

Section I. INTRODUCTION

C-1. Scope. This appendix lists integral components of and basic issue items for the SG-1223/T to help you inventory items required for safe and efficient operation.

C-2. General. This Components of End Item List is divided into the following sections:

a. Section II. Integral Components of the End Item. These items, when assembled, comprise the SG-1223/T and must accompany it whenever it is transferred or turned in. The illustrations will help you identify these items.

b. Section III. Basic Issue Items. These are the minimum essential items required to place the SG-1223/T in operation, to operate it, and to perform emergency repair. Although shipped separately packed they must accompany the SG-1223/T during operation and whenever it is transferred between accountable officers. The illustrations will assist you with hard-to-identify items. This manual is your authority to requisition replacement BII, based on TOE/MTOE authorization of the end item.

C-3. Explanation of Columns.

a. Illustration. This column is divided as follows:

(1) Figure Number. Indicates figure number of the illustration on which the item is shown.

(2) Item Number. The number used to identify item called out in the illustration.

b. National Stock Number. Indicates the National stock number assigned to the item and which will be used for requisitioning.

c. Part Number. Indicates the primary number used by the manufacturer, which controls the design and characteristics of the item by means of its engineering drawings, specifications, standards, and inspection requirements to identify an item or range of items.

d. Description. Indicates the Federal item name and, if required, a minimum description to identify the item.

e. Location. The physical location of each item listed is given in this column. The lists are designed to inventory all items in one area of the major item before moving on to an adjacent area.

f. Quantity Required (Qty Reqd). This column lists the quantity of each item required for a complete major item.

g. Quantity. This column is left blank for use during an inventory. Under the Recv'd column, list the quantity you actually receive on your major item. The Data columns are for your use when you inventory the major item at a later date; such as for shipment to another site.

SECTION II. INTEGRAL COMPONENTS OF END ITEM

(1) Illustration		(2)	(3)	(4)	(5)	(6)	(7)	(8) Quantity			
(a) Figure No.	(b) Item No.	National Stock Number	Part No.	Description	Location	Usable On Code	Qty Reqd	Rev'd	Date	Date	Date
C-1	1			Signal Generator SG-1223/T (80058)			1				

SECTION III.
BASIC ISSUE ITEMS

(1) ILLUSTRATION (a) FIGURE NO.	(1) ILLUSTRATION (b) ITEM NO.	(2) NATIONAL STOCK NUMBER	(3) PART NO.	(4) DESCRIPTION	(5) LOCATION	(6) USABLE ON CODE	(7) QTY REQD	(8) QUANTITY RCV'D	(8) QUANTITY DATE	(8) QUANTITY DATE	(8) QUANTITY DATE	(8) QUANTITY DATE
				NO BASIC ISSUE ITEMS								

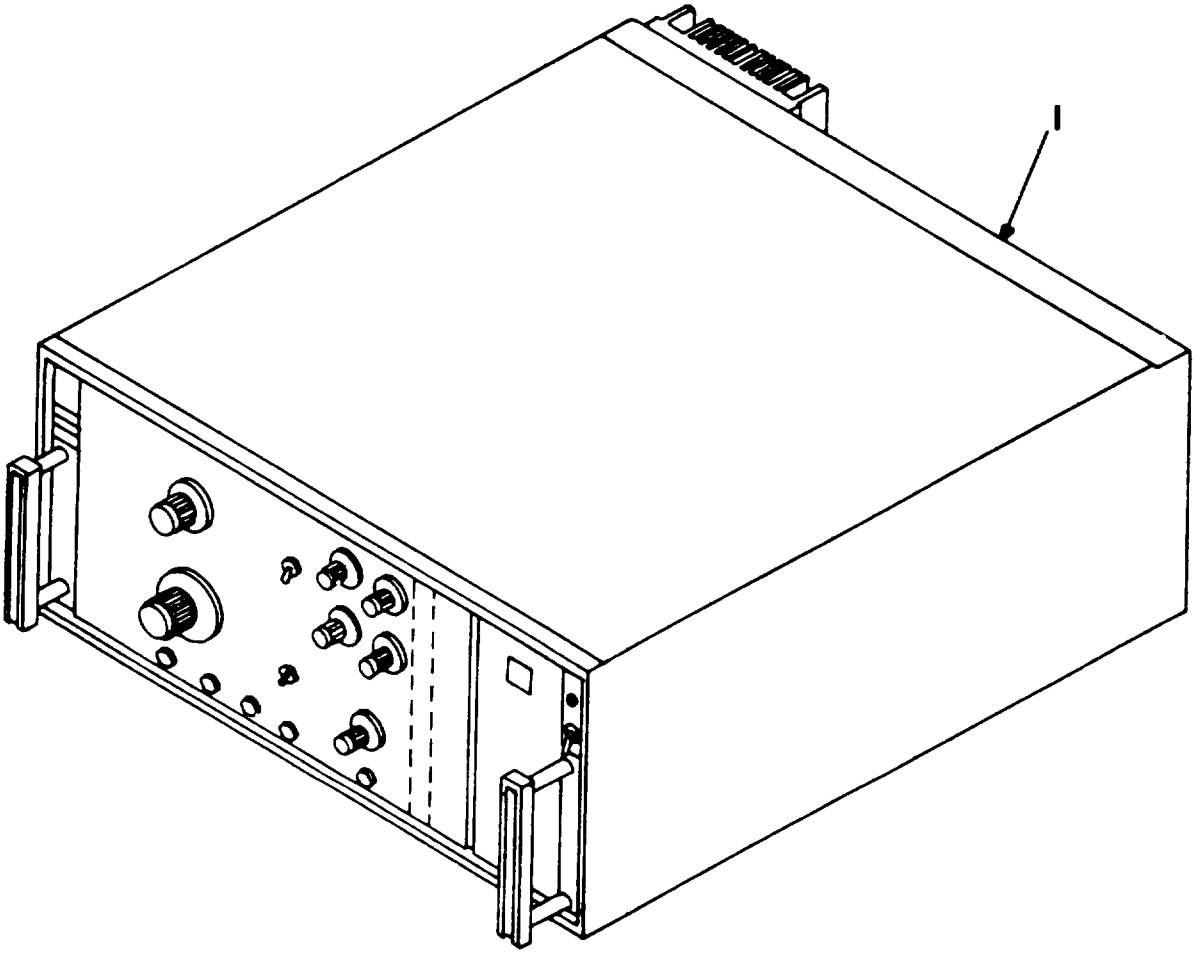


Figure C-1. Signal Generator SG-1223/T.

APPENDIX D

ADDITITIONAL AUTHORIZATION LIST

Section I. INTRODUCTION

D-1. Scope. This appendix lists additional items you are authorized for the support of the SG-1223/T.

D-2. General. This list identifies items that do not have to accompany the SG--1223/T and that do not have to be turned in with it. These items are all authorized to you by CTA, MTOE, TDA, or JTA.

D-3. Explanation of Listing. National stock numbers, deScriptions, and quantities are provided to help you identify and request the additional items you require to support this equipment.

Section II. ADDITIONAL AUTHORIZATION LIST

(1) NATIONAL STOCK NUMBER	(2) DESCRIPTION PART NUMBER & FSCM USABLE ON CODE	(3) U/M	(4) QTY AUTH
	NO ADDITIONAL AUTHORIZED ITEMS		

APPENDIX E

EXPENDABLE SUPPLIES AND MATERIALS LIST

Section I. INTRODUCTION

E-1. Scope. This appendix lists expendable supplies and materials you will need to operate and maintain the SG-1223/T. These items are authorized to you by CTA 50-970, Expendable Items (Except Medical, Class V, Repair Parts, and Heraldic Items).

E-2. Explanation of Columns.

a. Column 1 - Item Number. This number is assigned to the entry in the listing and is referenced in the narrative instructions to identify the material (e.g., "Use cleaning compound, item 5, App. D").

b. Column 2 - Level. This column identifies the lowest level of maintenance that requires the listed item.

C - Operator/Crew
O - Organizational Maintenance
F - Direct Support Maintenance
H - General Support Maintenance

c. Column 3 - National Stock Number. This is the National stock number assigned to the item; use it to request or requisition the item.

d. Column 4 - Description. Indicates the Federal item name and, if required, a description to identify the item. The last line for each item indicates the part number followed by the Federal Supply Code for Manufacturer (FSCM) in parentheses, if applicable.

e. Column 5 - Unit of Measure (U/M). Indicates the measure used in performing the actual maintenance function. This measure is expressed by a two-character alphabetical abbreviation (e.g., ea, in, pr). If the unit of measure differs from the unit of issue, requisition the lowest unit of issue that will satisfy your requirements.

(1) ITEM NUMBER	(2) LEVEL	(3) NATIONAL STOCK NUMBER	(4) DESCRIPTION	(5) U/M
1	0	8305-267-3015	Cloth, cotton, cheesecloth	ROLL
2	0		Enamel	QT
3	0	8010-582-5318	Primer, zinc chromate	QT
4	0		Sandpaper, Fine, No. 0000	SHT
5	0		Soft-bristle brush	EA
6	0	6810-00-292-9625	Trichlorotrifluoroethane 0T620 (81349)	OZ

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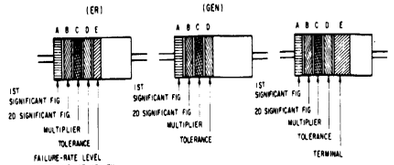


COLOR CODE MARKING FOR COMPOSITION TYPE RESISTORS

COLOR-CODE MARKING FOR FILM-TYPE RESISTORS

TABLE I
COLOR CODE FOR COMPOSITION TYPE AND FILM TYPE RESISTORS

BAND A		BAND B		BAND C		BAND D		BAND E		
COLOR	FIRST SIGNIFICANT FIGURE	COLOR	SECOND SIGNIFICANT FIGURE	COLOR	MULTIPLIER	COLOR	RESISTANCE TOLERANCE (PERCENT)	COLOR	FAILURE RATE LEVEL	TERM
BLACK	0	BLACK	0	BLACK	1			BROWN	M=1.0	
BROWN	1	BROWN	1	BROWN	10			RED	P=0.1	
RED	2	RED	2	RED	100			ORANGE	R=0.01	
ORANGE	3	ORANGE	3	ORANGE	1,000			YELLOW	S=0.001	
YELLOW	4	YELLOW	4	YELLOW	10,000	SILVER	±10 (COMP TYPE ONLY)	WHITE		SOLDERABLE
GREEN	5	GREEN	5	GREEN	100,000	GOLD	±5			
BLUE	6	BLUE	6	BLUE	1,000,000	RED	±2 (NOT APPLICABLE TO ESTABLISHED RELIABILITY)			
PURPLE (VIOLET)	7	PURPLE (VIOLET)	7							
GRAY	8	GRAY	8	SILVER	0.01					
WHITE	9	WHITE	9	GOLD	0.1					

BAND A — THE FIRST SIGNIFICANT FIGURE OF THE RESISTANCE VALUE (BANDS A THRU D SHALL BE OF EQUAL WIDTH)

BAND B — THE SECOND SIGNIFICANT FIGURE OF THE RESISTANCE VALUE

BAND C — THE MULTIPLIER (THE MULTIPLIER IS THE FACTOR BY WHICH THE TWO SIGNIFICANT FIGURES ARE MULTIPLIED TO YIELD THE NOMINAL RESISTANCE VALUE.)

BAND D — THE RESISTANCE TOLERANCE

BAND E — WHEN USED ON COMPOSITION RESISTORS, BAND E INDICATES ESTABLISHED RELIABILITY FAILURE-RATE LEVEL (PERCENT FAILURE PER 1,000 HOURS). ON FILM RESISTORS, THIS BAND SHALL BE APPROXIMATELY 1-1/2 TIMES THE WIDTH OF OTHER BANDS AND INDICATES TYPE OF TERMINAL.

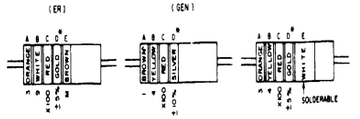
RESISTANCES IDENTIFIED BY NUMBERS AND LETTERS (THESE ARE NOT COLOR CODED.)

SOME RESISTORS ARE IDENTIFIED BY THREE OR FOUR DIGIT ALPHA NUMERIC DESIGNATORS. THE LETTER R IS USED IN PLACE OF A DECIMAL POINT WHEN FRACTIONAL VALUES OF AN OHM ARE EXPRESSED. FOR EXAMPLE:

2R7 = 2.7 OHMS 10R0 = 10.0 OHMS

FOR WIRE-WOUND-TYPE RESISTORS COLOR CODING IS NOT USED. IDENTIFICATION MARKING IS SPECIFIED IN EACH OF THE APPLICABLE SPECIFICATIONS.

EXAMPLES OF COLOR CODING



NOMINAL RESISTANCE 3,900 OHMS
RESISTANCE TOLERANCE ±5%
FAILURE RATE LEVEL M

NOMINAL RESISTANCE 1,400 OHMS
RESISTANCE TOLERANCE ±10%

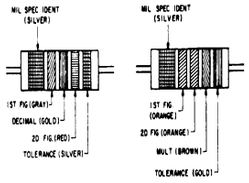
NOMINAL RESISTANCE 3,400 OHMS
RESISTANCE TOLERANCE ±5%
TERMINAL, SOLDERABLE

COMPOSITION-TYPE RESISTORS

FILM-TYPE RESISTORS

* IF BAND D IS OMITTED, THE RESISTOR TOLERANCE IS ±20% AND THE RESISTOR IS NOT MIL-STD.

A. COLOR CODE MARKING FOR MILITARY STANDARD RESISTORS



(A) 8.2 UH ± 10% (B) 330 UH ± 5%

COLOR CODING FOR TUBULAR ENCAPSULATED R.F. CHOKES. AT A, AN EXAMPLE OF THE CODING FOR AN 8.2 UH CHOKE IS GIVEN. AT B, THE COLOR BANDS FOR A 330 UH INDUCTOR ARE ILLUSTRATED

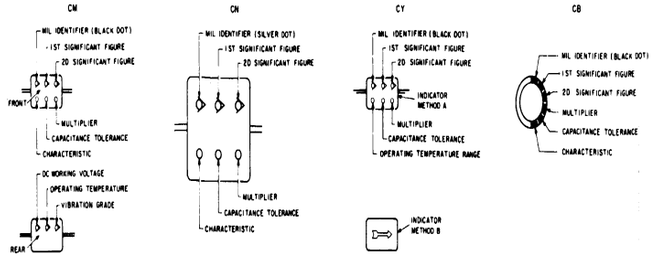
TABLE 2
COLOR CODING FOR TUBULAR ENCAPSULATED R.F. CHOKES.

COLOR	SIGNIFICANT FIGURE	MULTIPLIER	INDUCTANCE TOLERANCE (PERCENT)
BLACK	0	1	
BROWN	1	10	1
RED	2	100	2
ORANGE	3	1,000	3
YELLOW	4		
GREEN	5		
BLUE	6		
VIOLET	7		
GRAY	8		
WHITE	9		
NONE			20
SILVER			10
GOLD	DECIMAL POINT		5

MULTIPLIER IS THE FACTOR BY WHICH THE TWO COLOR FIGURES ARE MULTIPLIED TO OBTAIN THE INDUCTANCE VALUE OF THE CHOKE COIL

B. COLOR CODE MARKING FOR MILITARY STANDARD INDUCTORS.

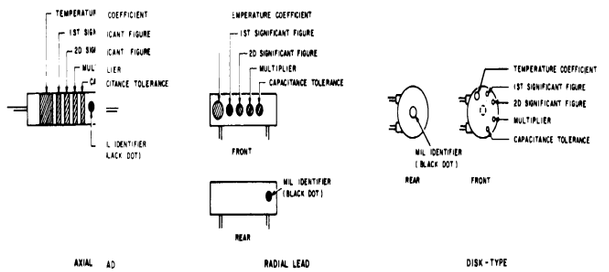
CAPACITORS, FIXED, VARIOUS-DIELECTRICS, STYLES CM, CN, CY, AND CB



MICA-DIELECTRIC PAPER-DIELECTRIC GLASS-DIELECTRIC, GLASS CASE MICA, BUTTON TYPE

TABLE 3 — FOR USE WITH STYLES CM, CN, CY AND CB

COLOR	MIL ID	1ST SIG FIG	2D SIG FIG	MULTIPLIER	CAPACITANCE TOLERANCE				CHARACTERISTIC			DC WORKING VOLTAGE	OPERATING TEMP RANGE	VIBRATION GRADE
					CM	CN	CY	CB	CM	CN	CB	CM	CX, CM	CM
BLACK	CM, CY, CB	0	0	1			±20%	±20%	A				-55°TO+70°C	10-55 HZ
BROWN		1	1	10					B	E	B			
RED		2	2	100	±2%		±2%	±2%	C				-55°TO+85°C	
ORANGE		3	3	1,000	±30%				D		D	300		
YELLOW		4	4	10,000					E				-55°TO+125°C	10-2,000 HZ
GREEN		5	5		±5%				F			500		
BLUE		6	6										-55°TO+150°C	
PURPLE (VIOLET)		7	7											
GRAY		8	8											
WHITE		9	9											
GOLD				0.1			±5%	±5%						
SILVER	CN			0.01	±10%	±10%	±10%	±10%						



AXIAL RADIAL LEAD DISK-TYPE

C. COLOR CODE MARKING FOR MILITARY STANDARD CAPACITORS

TABLE 4 — TEMPERATURE COMPENSATING, STYLE CC

COLOR	TEMPERATURE COEFFICIENT	1ST SIG FIG	2D SIG FIG	MULTIPLIER	CAPACITANCE TOLERANCE		MIL ID
					CAPACITANCES OVER 10 UUF	CAPACITANCES 10 UUF OR LESS	
BLACK	0	0	0	1		±1.0 UUF	CC
BROWN	-30	1	1	10	±1%		
RED	-80	2	2	100	±2%	±0.25 UUF	
ORANGE	-150	3	3	1,000			
YELLOW	-220	4	4				
GREEN	-330	5	5		±5%	±0.5 UUF	
BLUE	-470	6	6				
PURPLE (VIOLET)	-750	7	7				
GRAY		8	8	0.01*			
WHITE		9	9	0.1*	±10%		
GOLD	+100			0.1		±1.0 UUF	
SILVER				0.01			

1. THE MULTIPLIER IS THE NUMBER BY WHICH THE TWO SIGNIFICANT (SIG) FIGURES ARE MULTIPLIED TO OBTAIN THE CAPACITANCE IN UUF.

2. LETTERS INDICATE THE CHARACTERISTICS DESIGNATED IN APPLICABLE SPECIFICATIONS MIL-C-5, MIL-C-250, MIL-C-11272B, AND MIL-C-10950C RESPECTIVELY.

3. LETTERS INDICATE THE TEMPERATURE RANGE AND VOLTAGE-TEMPERATURE LIMITS DESIGNATED IN MIL-C-11015D.

4. TEMPERATURE COEFFICIENT IN PARTS PER MILLION PER DEGREE CENTIGRADE.

* OPTIONAL CODING WHERE METALLIC PIGMENTS ARE UNDESIRABLE.

9445-82

Figure FO-1. Standard Color Coding Chart

Figure FO-1. Standard Color Coding Chart

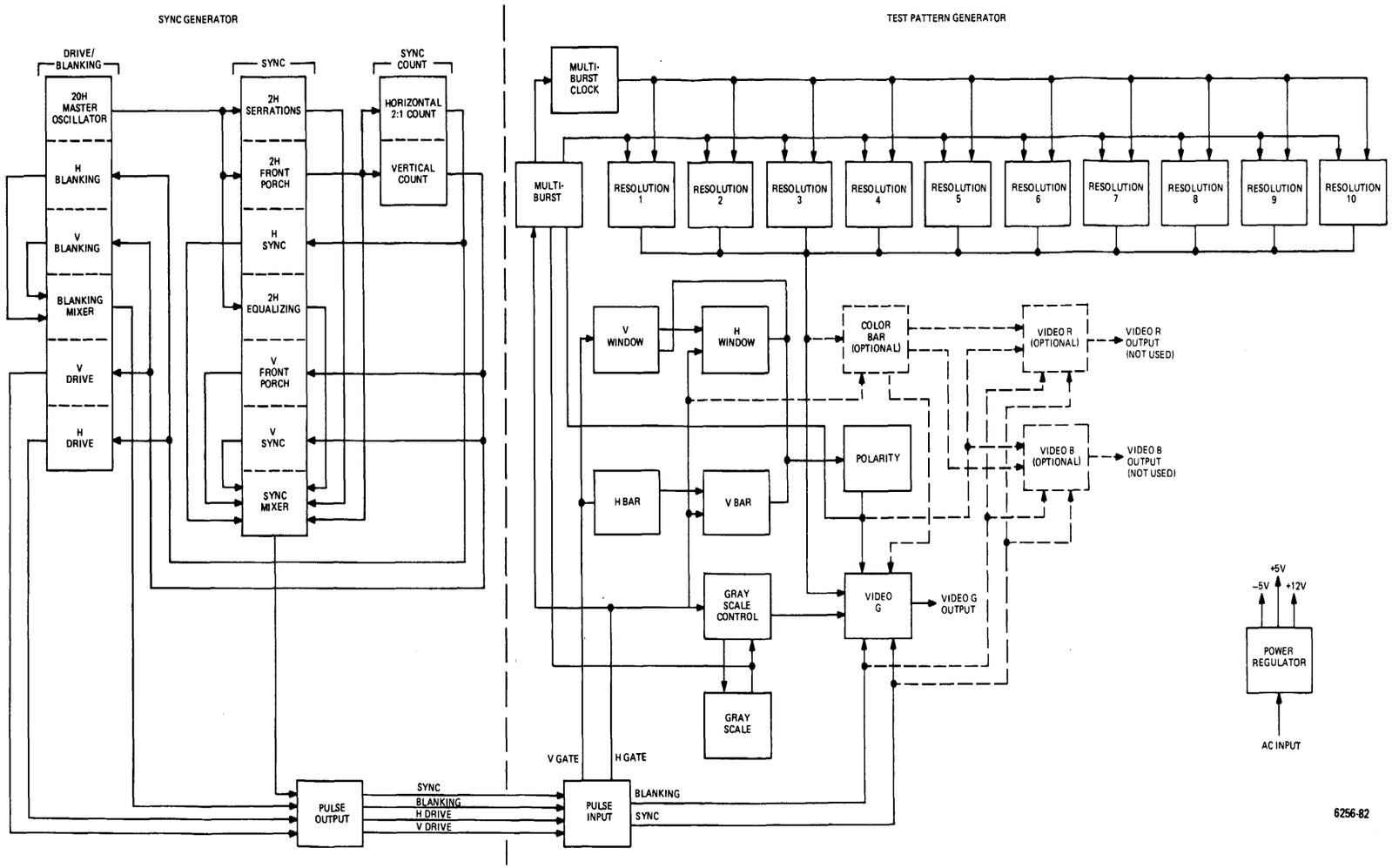


Figure FO-2. Test Pattern Generator, Functional Block Diagram

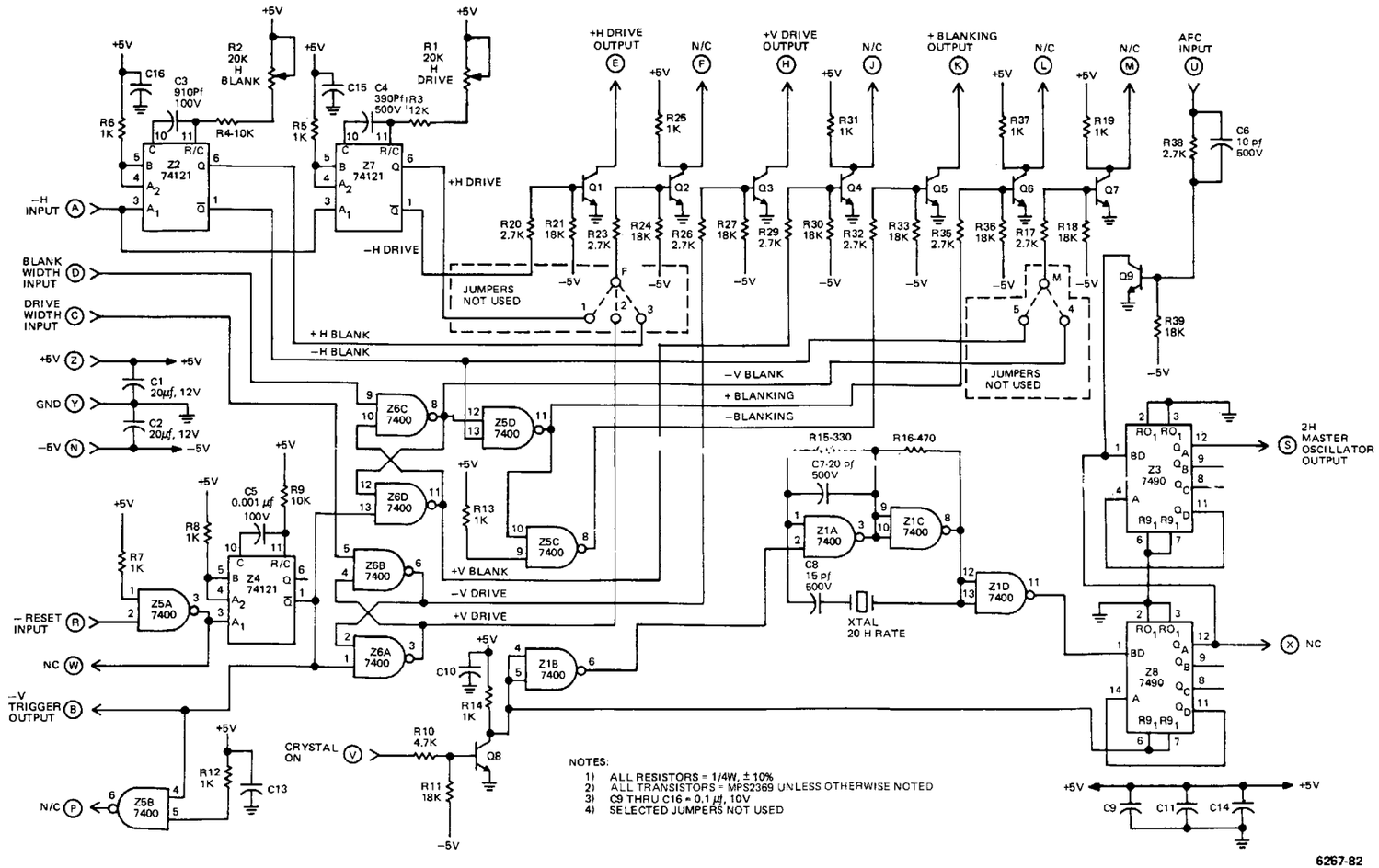


Figure FO-3. Drive/Blanking Schematic Diagram

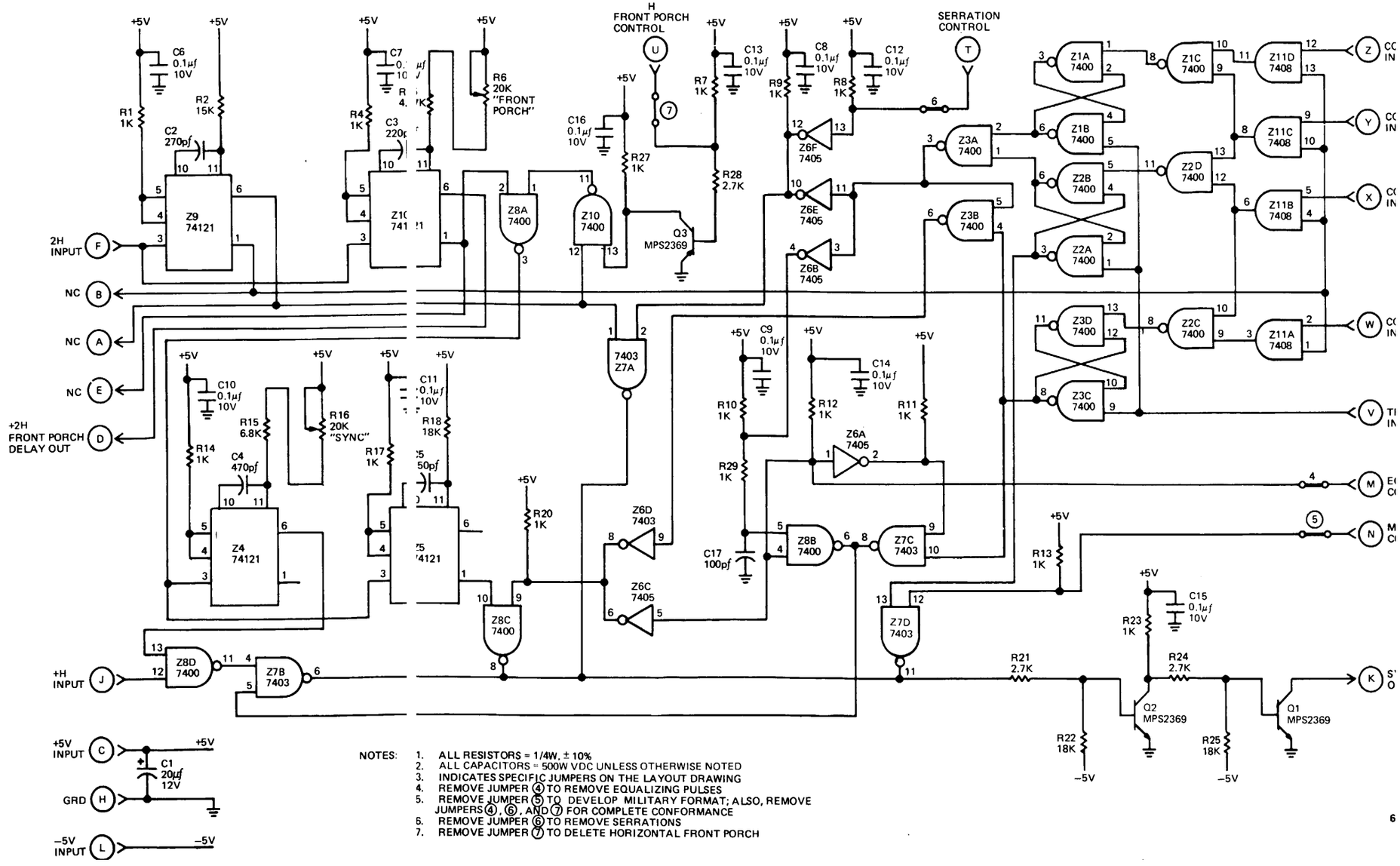


Figure FO-4. Sync Schematic Diagram

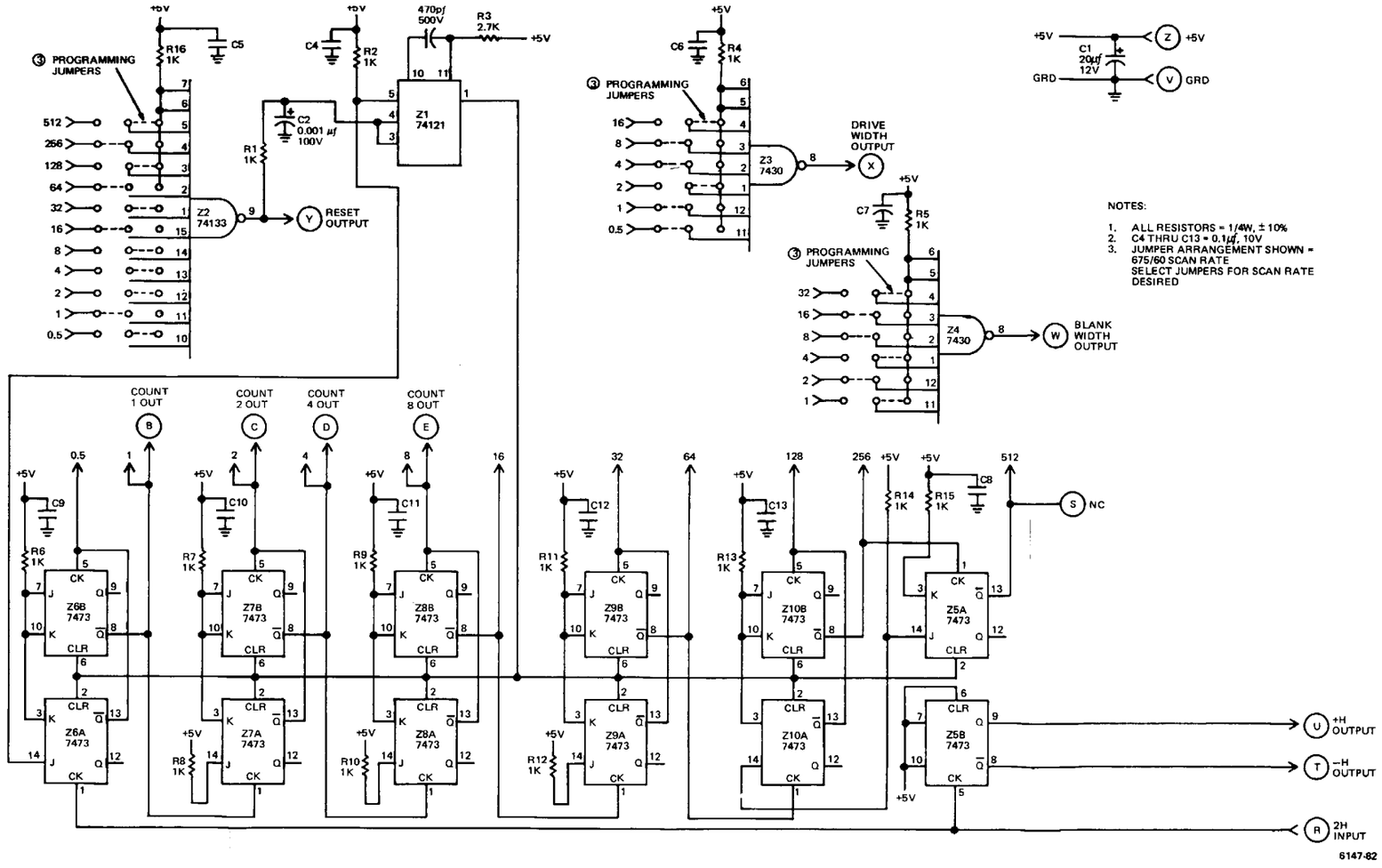


Figure FO-5. Sync Count Schematic Diagram

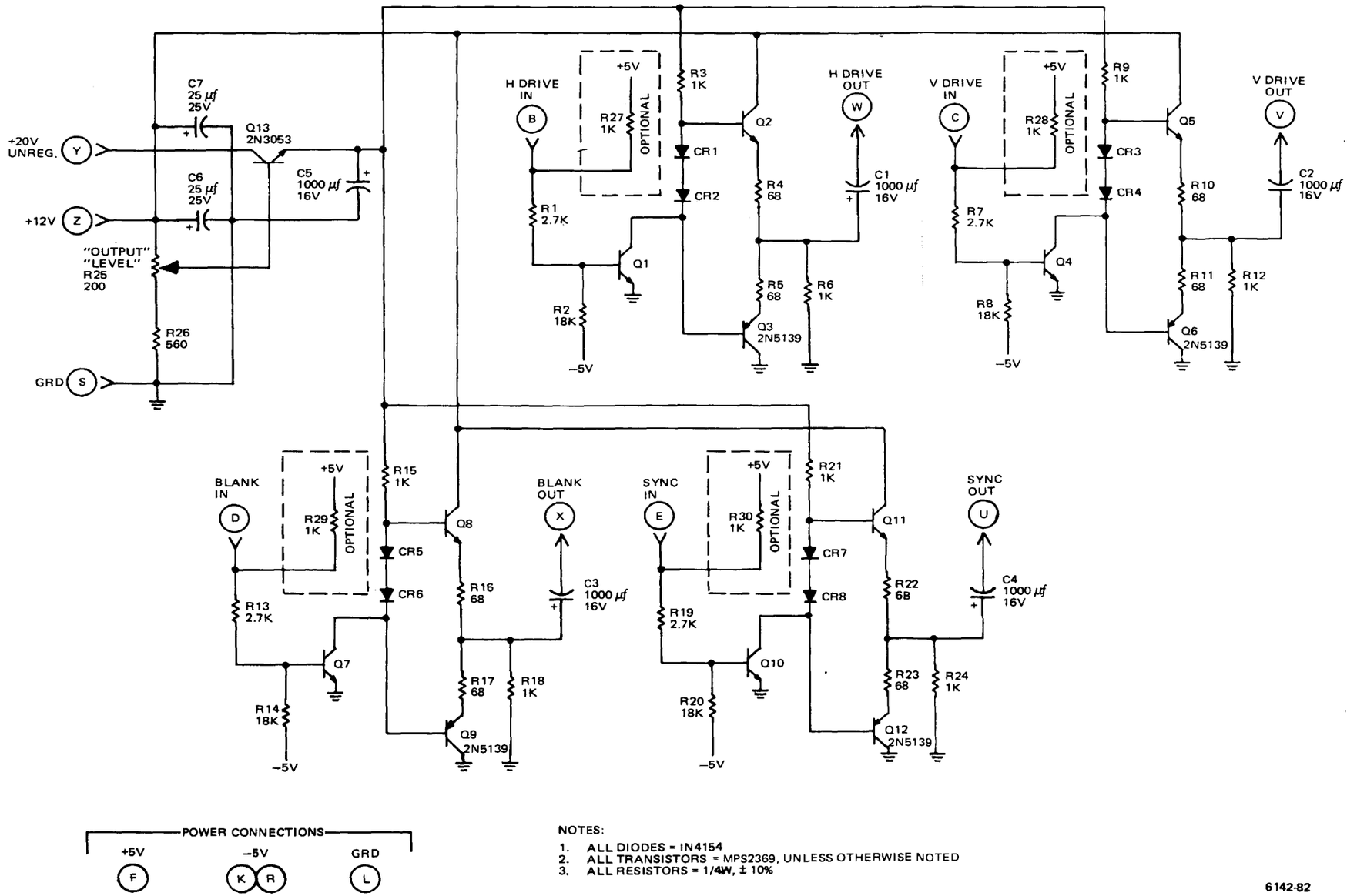


Figure FO-6. Pulse Output Schematic Diagram

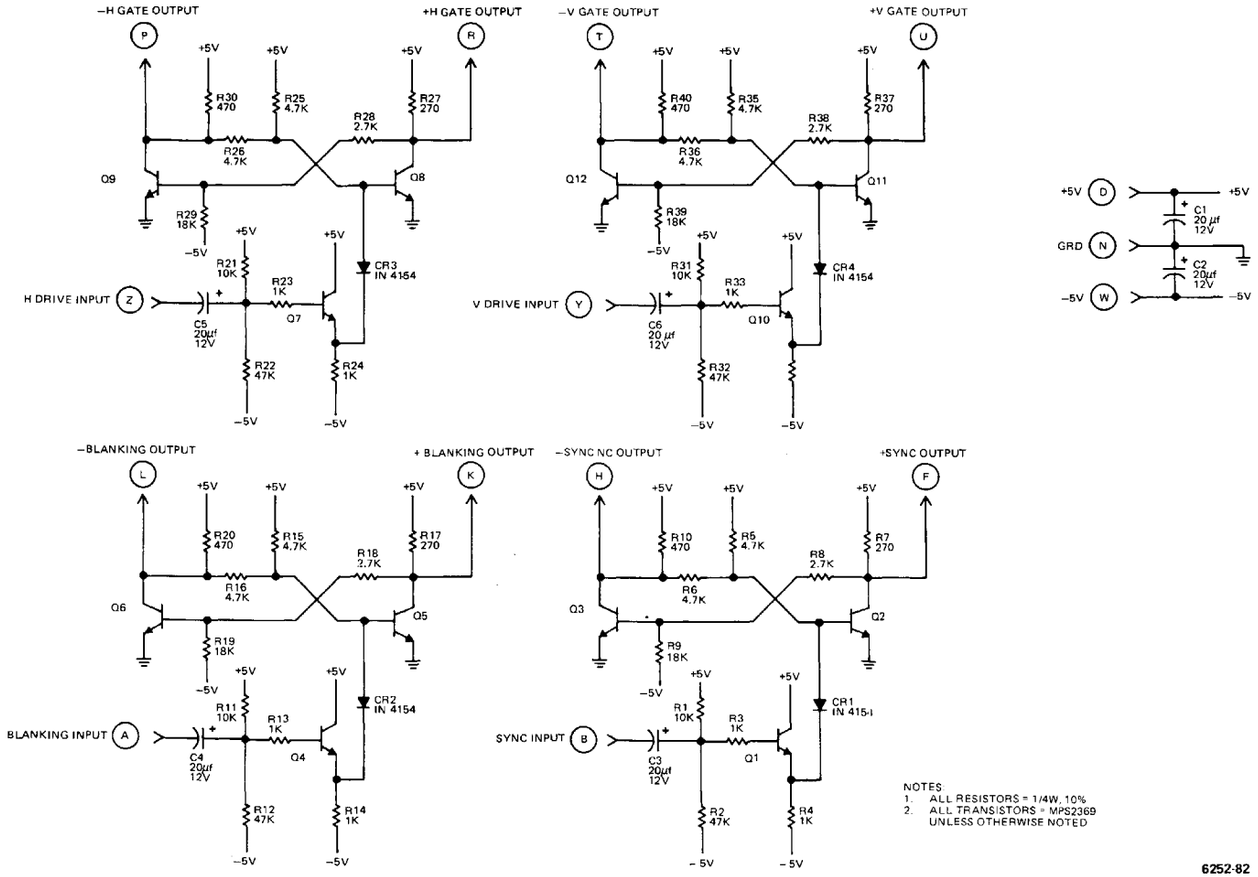


Figure FO-7. Pulse Input Schematic Diagram

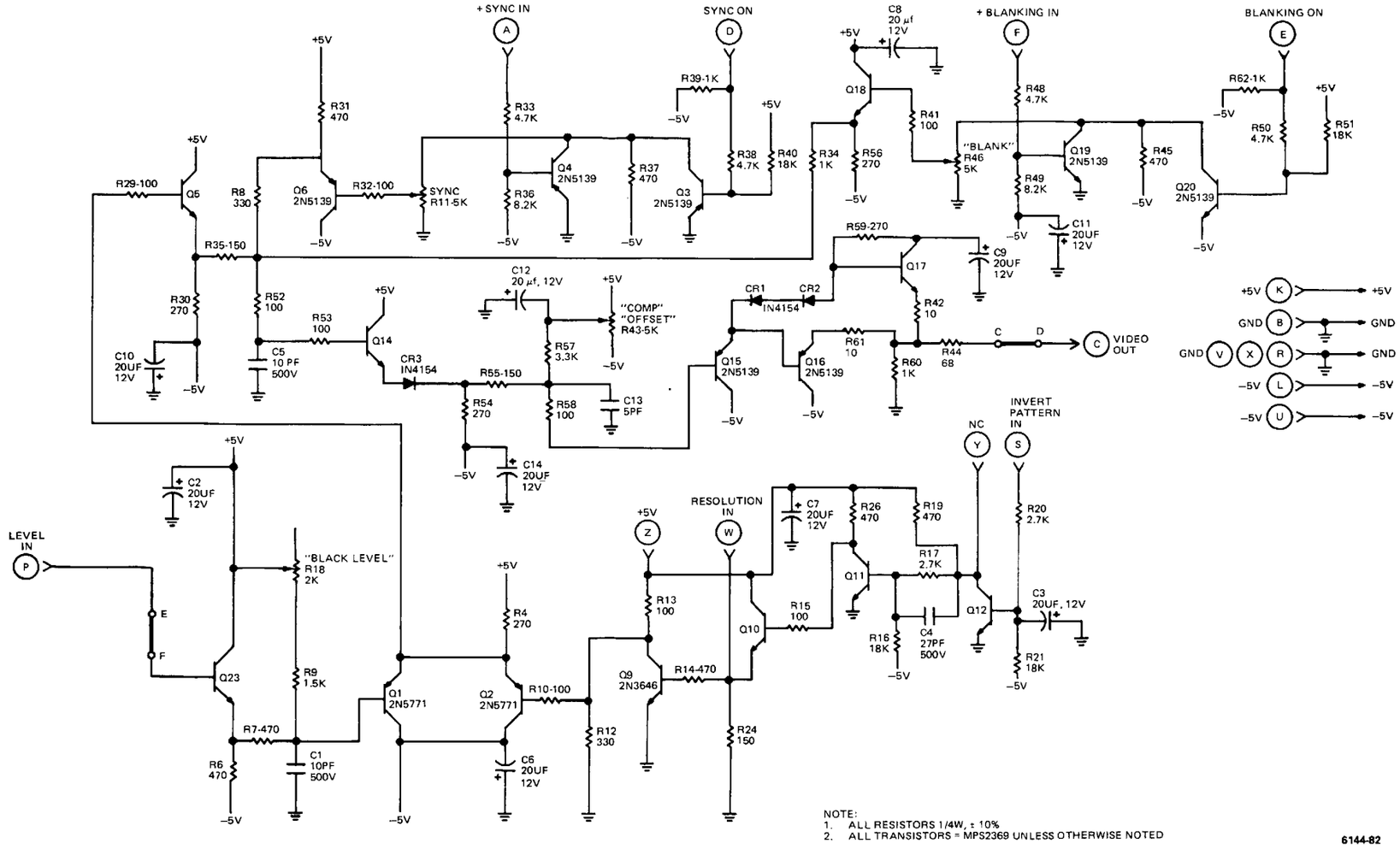
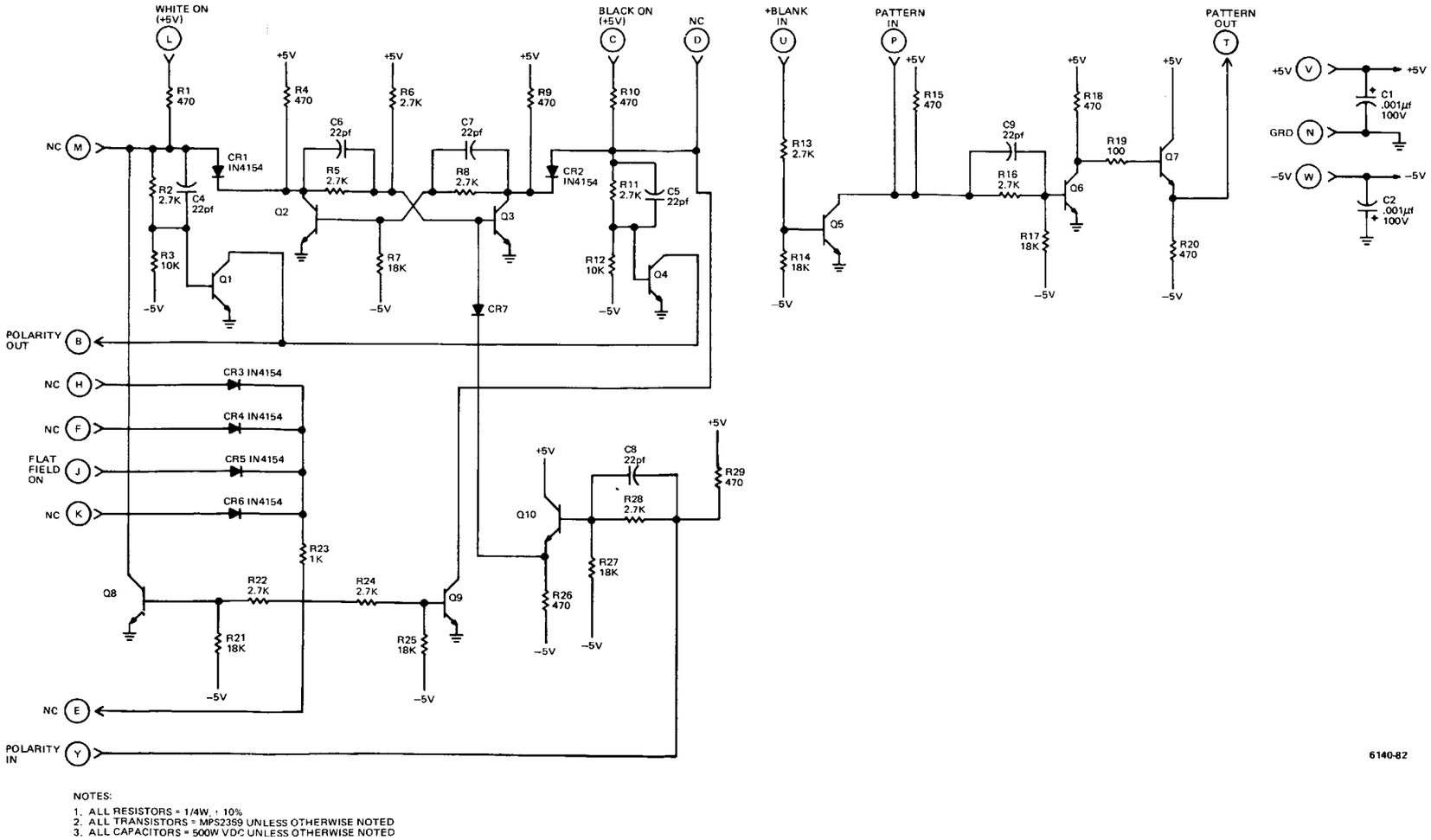


Figure FO-8. Video Schematic Diagram



NOTES:
1. ALL RESISTORS = 1/4W, ± 10%
2. ALL TRANSISTORS = MPS2369 UNLESS OTHERWISE NOTED
3. ALL CAPACITORS = 500W VDC UNLESS OTHERWISE NOTED

Figure FO-9. Polarity Schematic Diagram

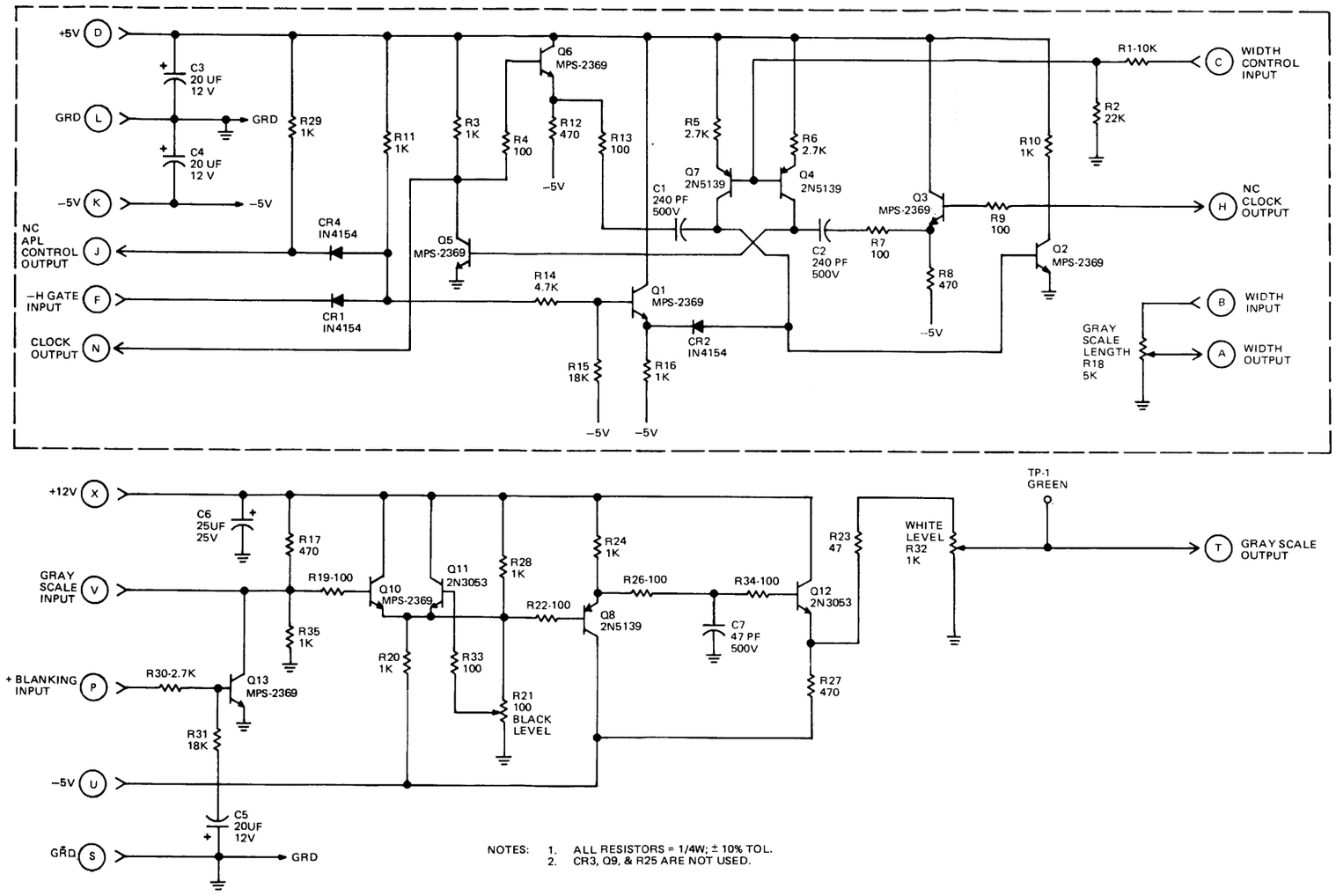


Figure FO-10. Gray Scale Control Schematic Diagram

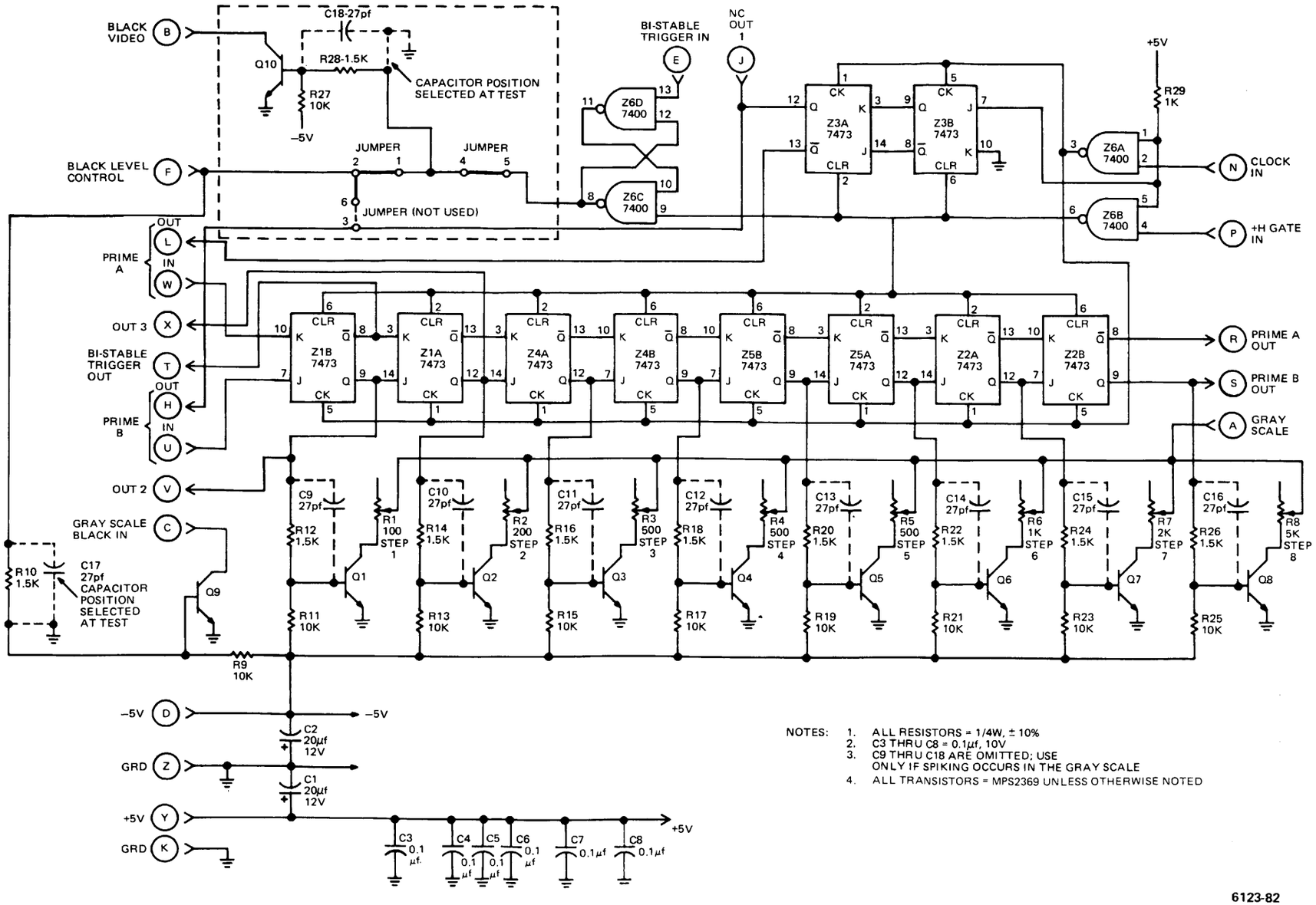


Figure FO-11. Gray Scale Schematic Diagram

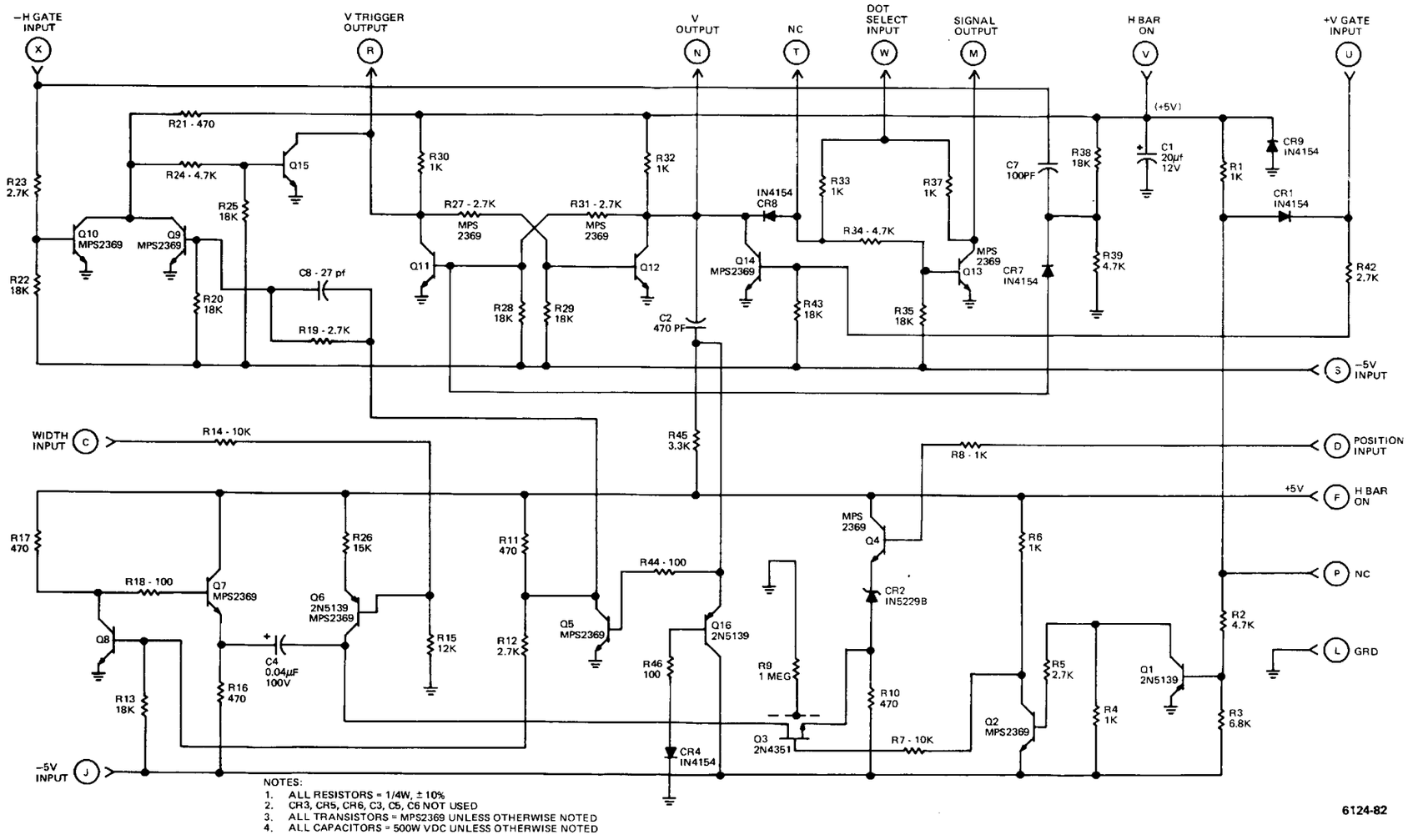
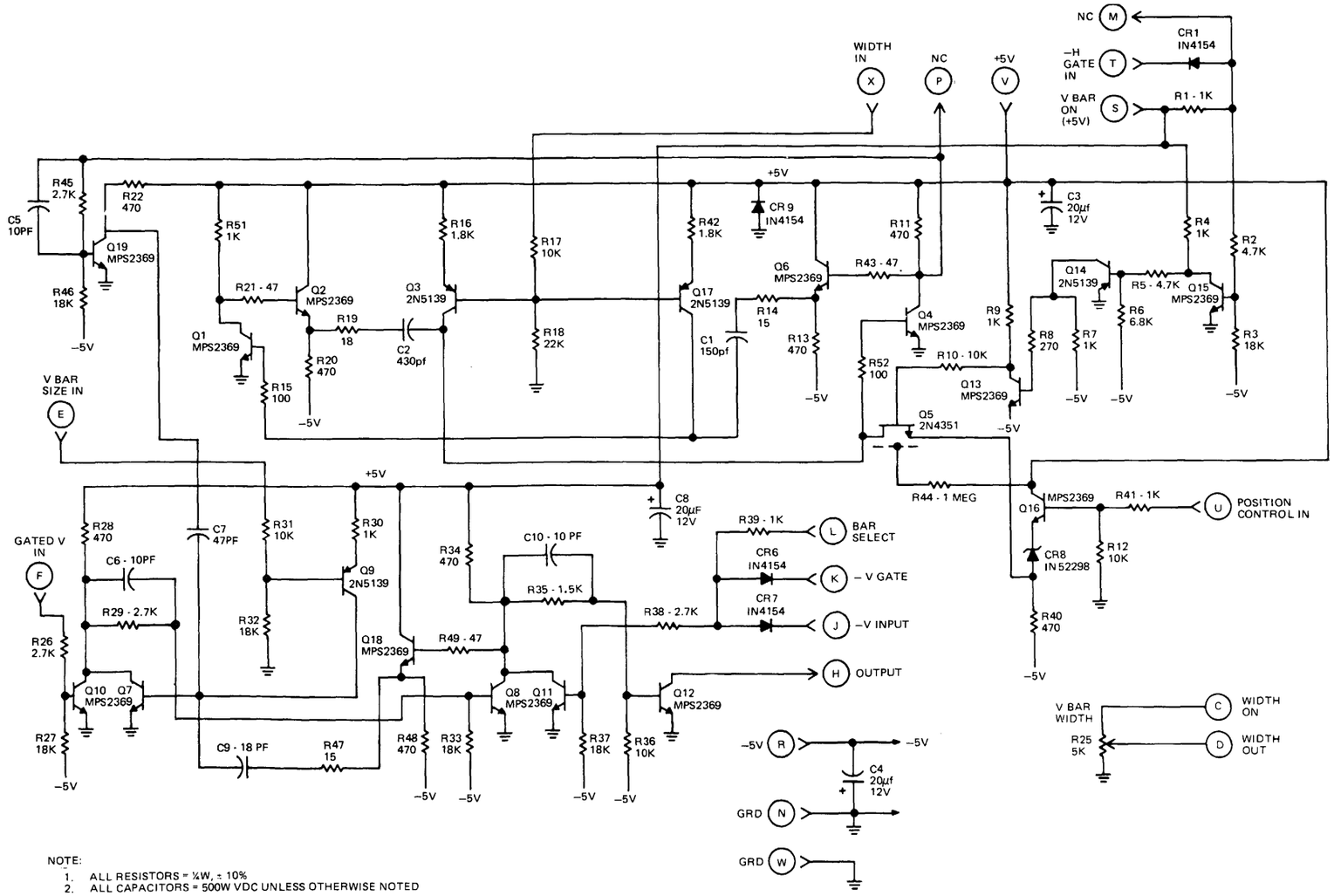


Figure FO-12. H Bar Schematic Diagram



NOTE:
1. ALL RESISTORS = ¼W, ± 10%
2. ALL CAPACITORS = 500W VDC UNLESS OTHERWISE NOTED

Figure FO-13. V Bar Schematic Diagram

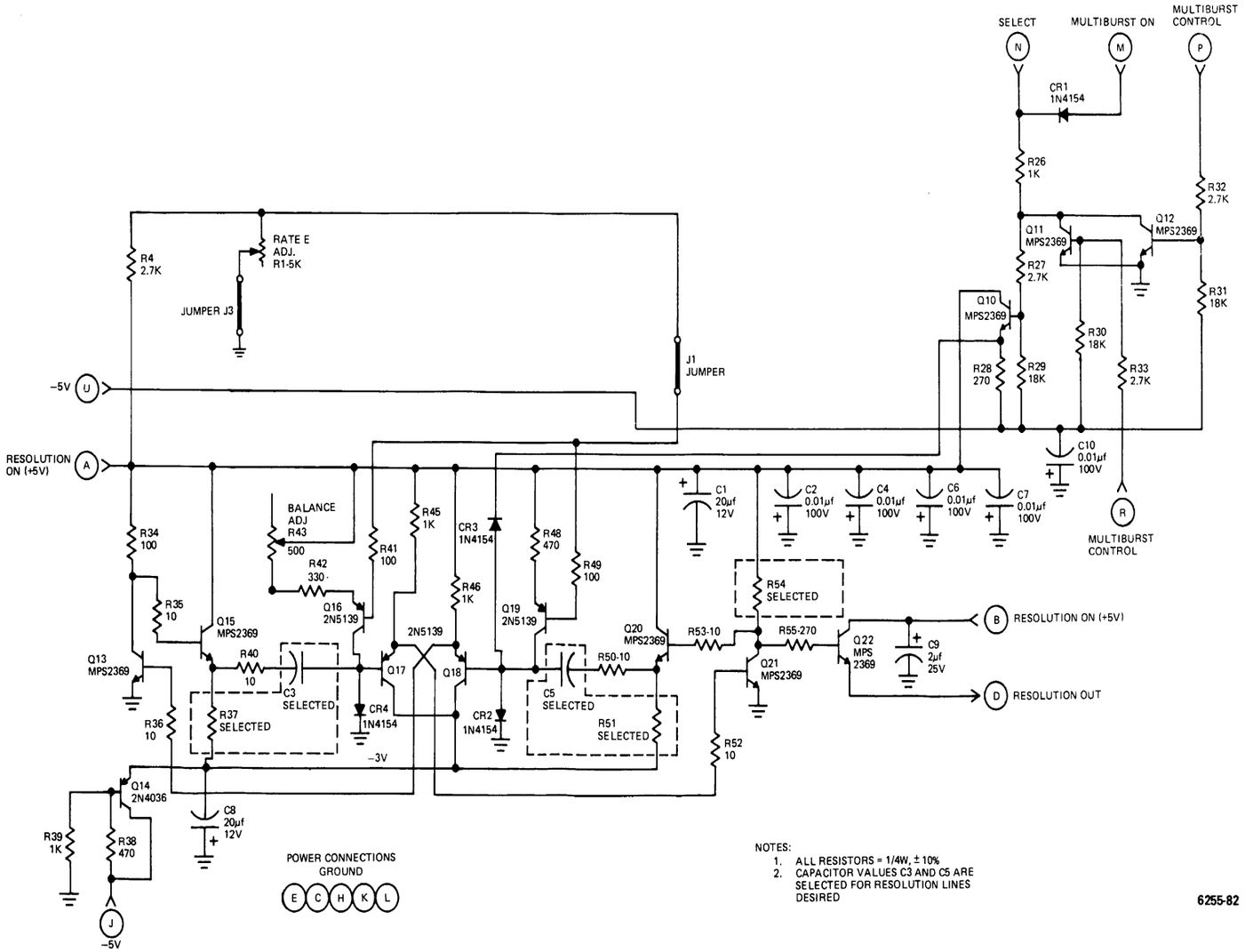


Figure FO-14. Resolution Schematic Diagram

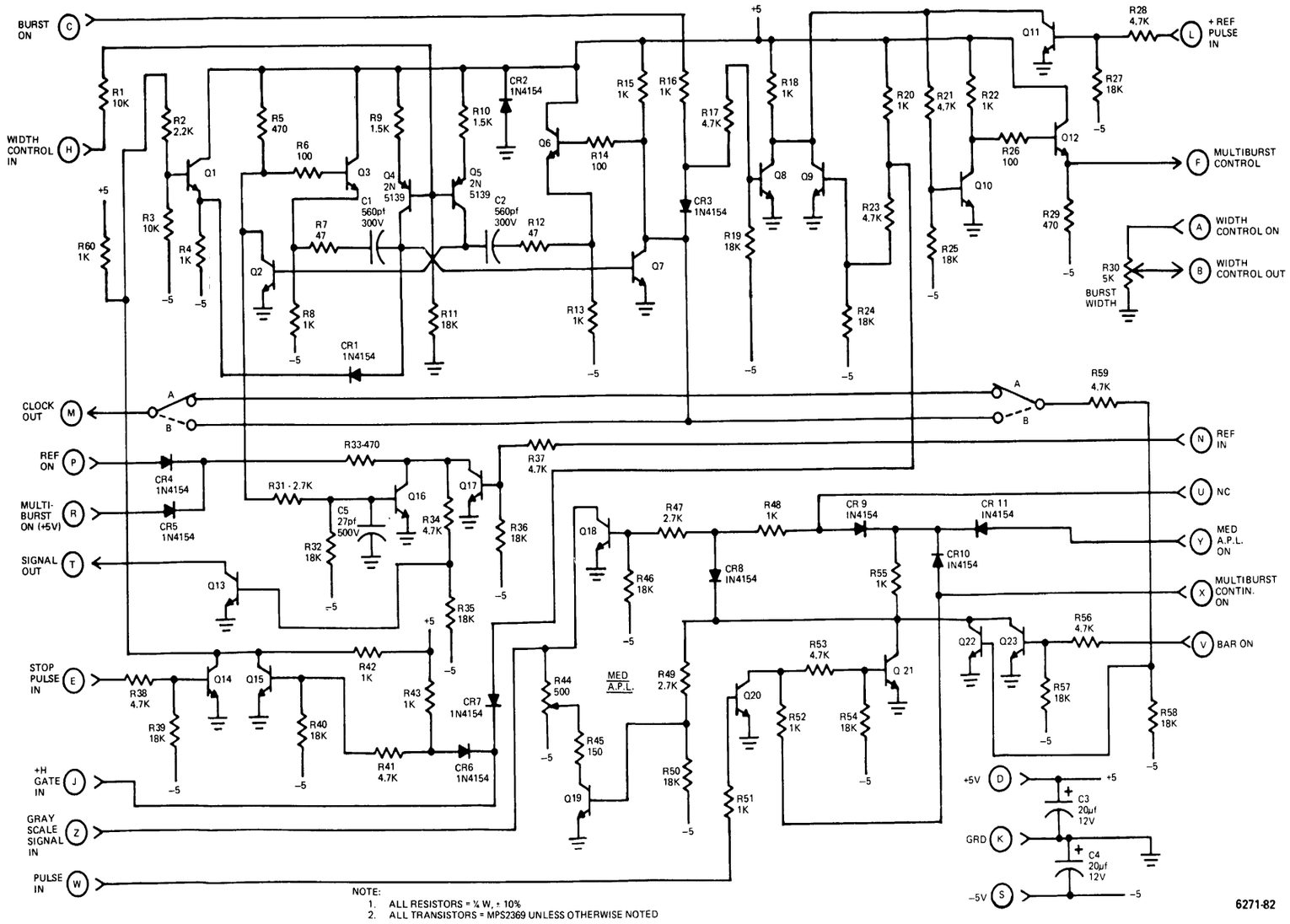


Figure FO-15. Multiburst Schematic Diagram

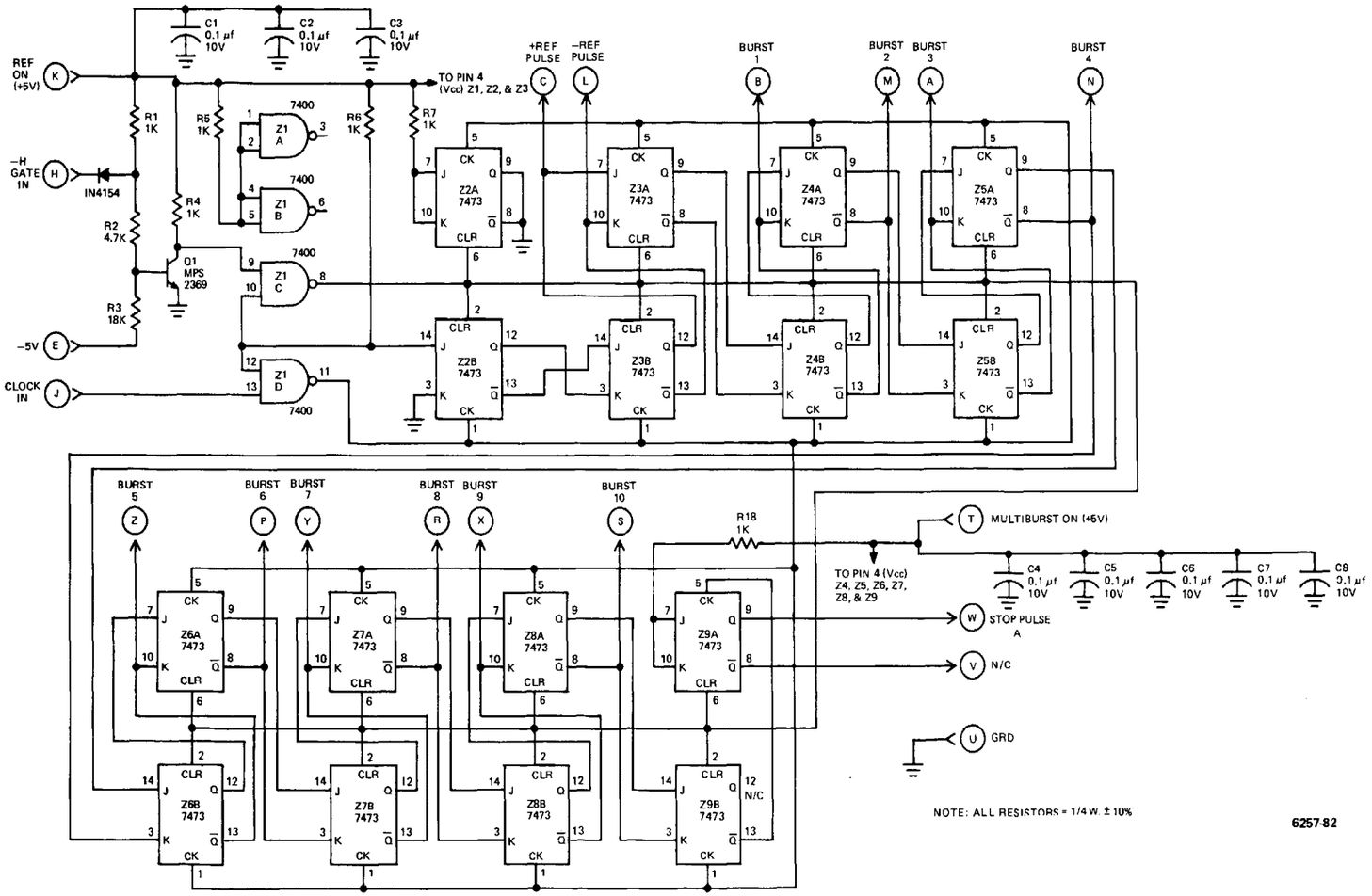


Figure FO-16. Multiburst Clock Schematic Diagram

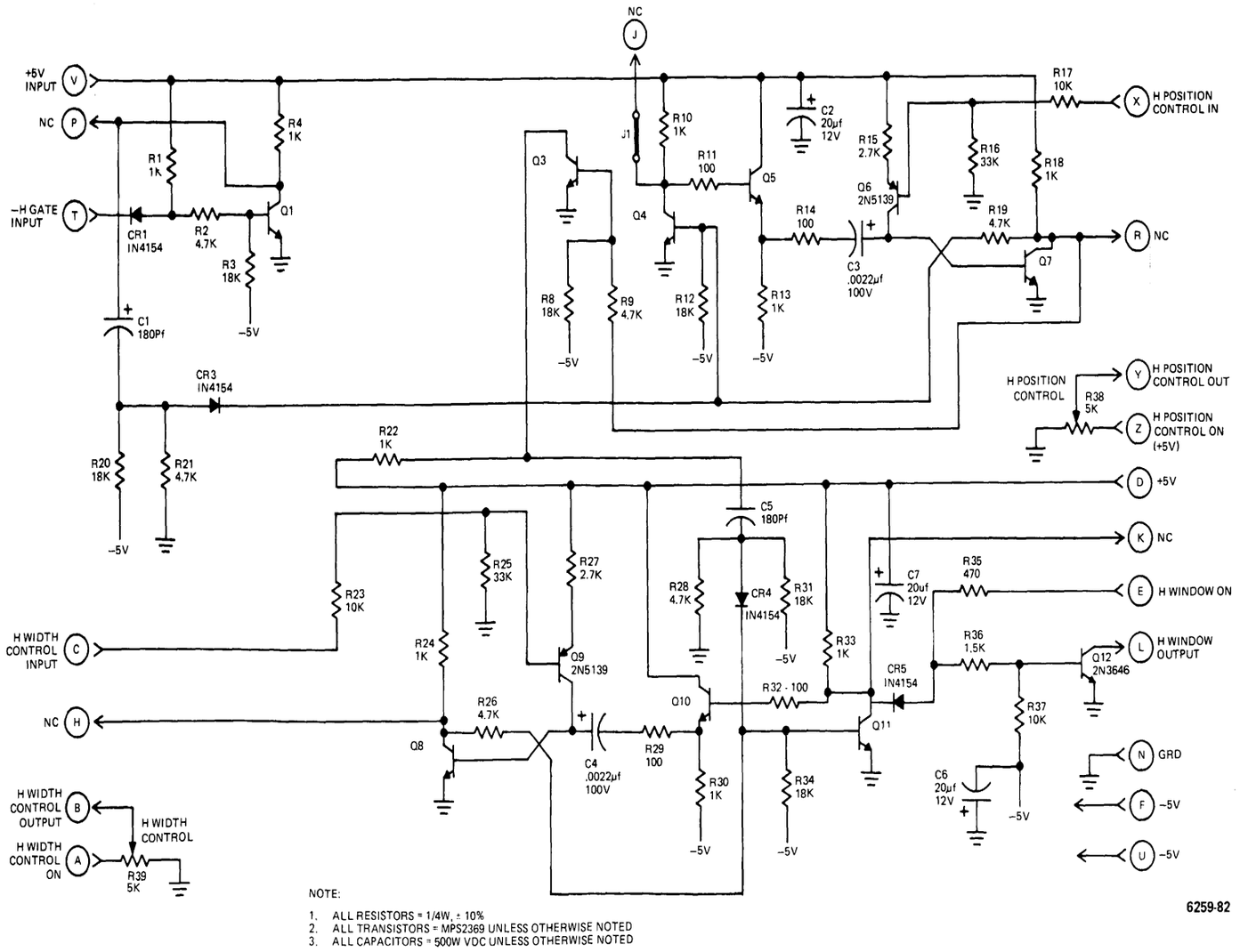


Figure FO-17. H Window Schematic Diagram

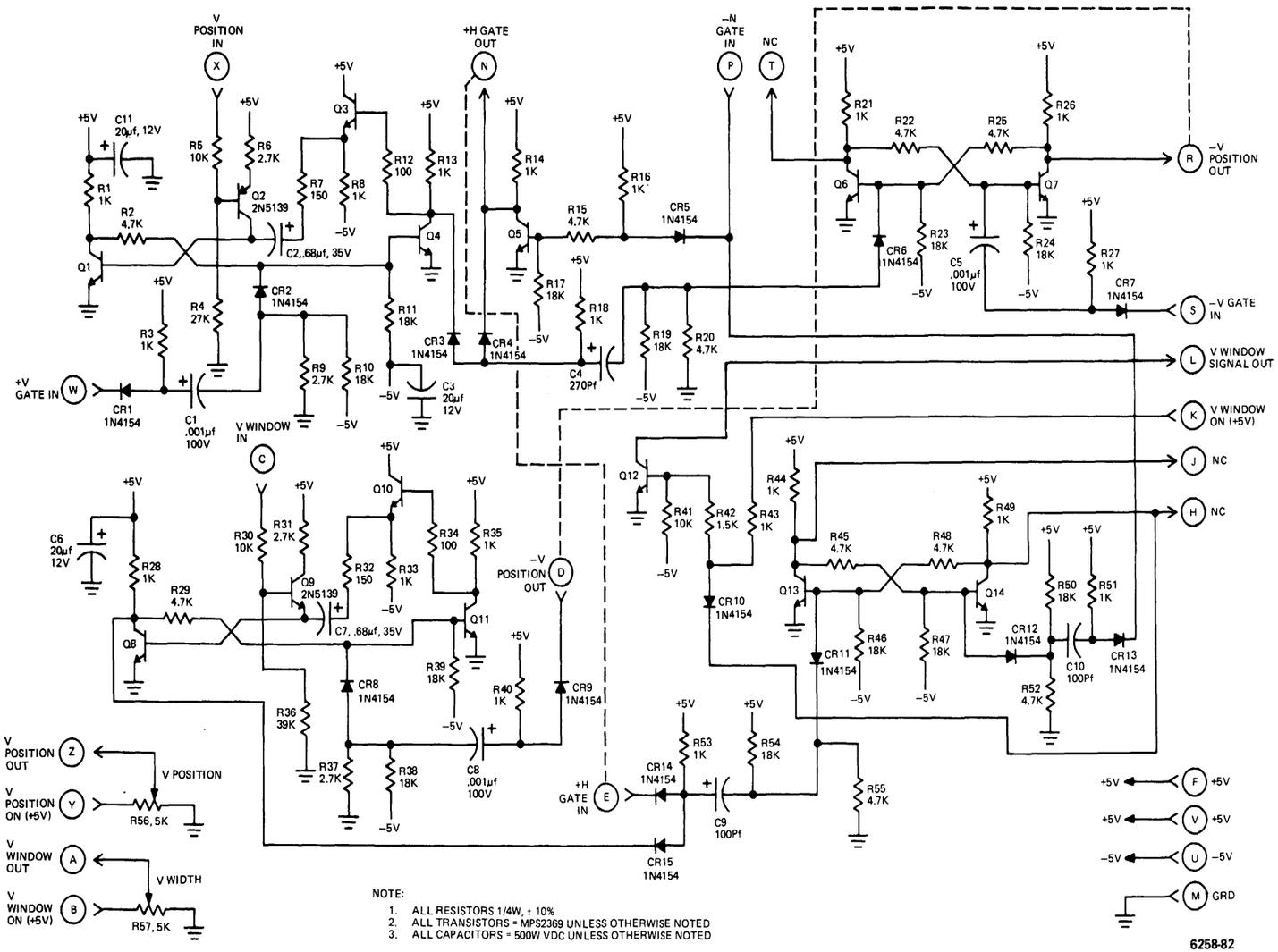


Figure FO-18. V Window Schematic Diagram

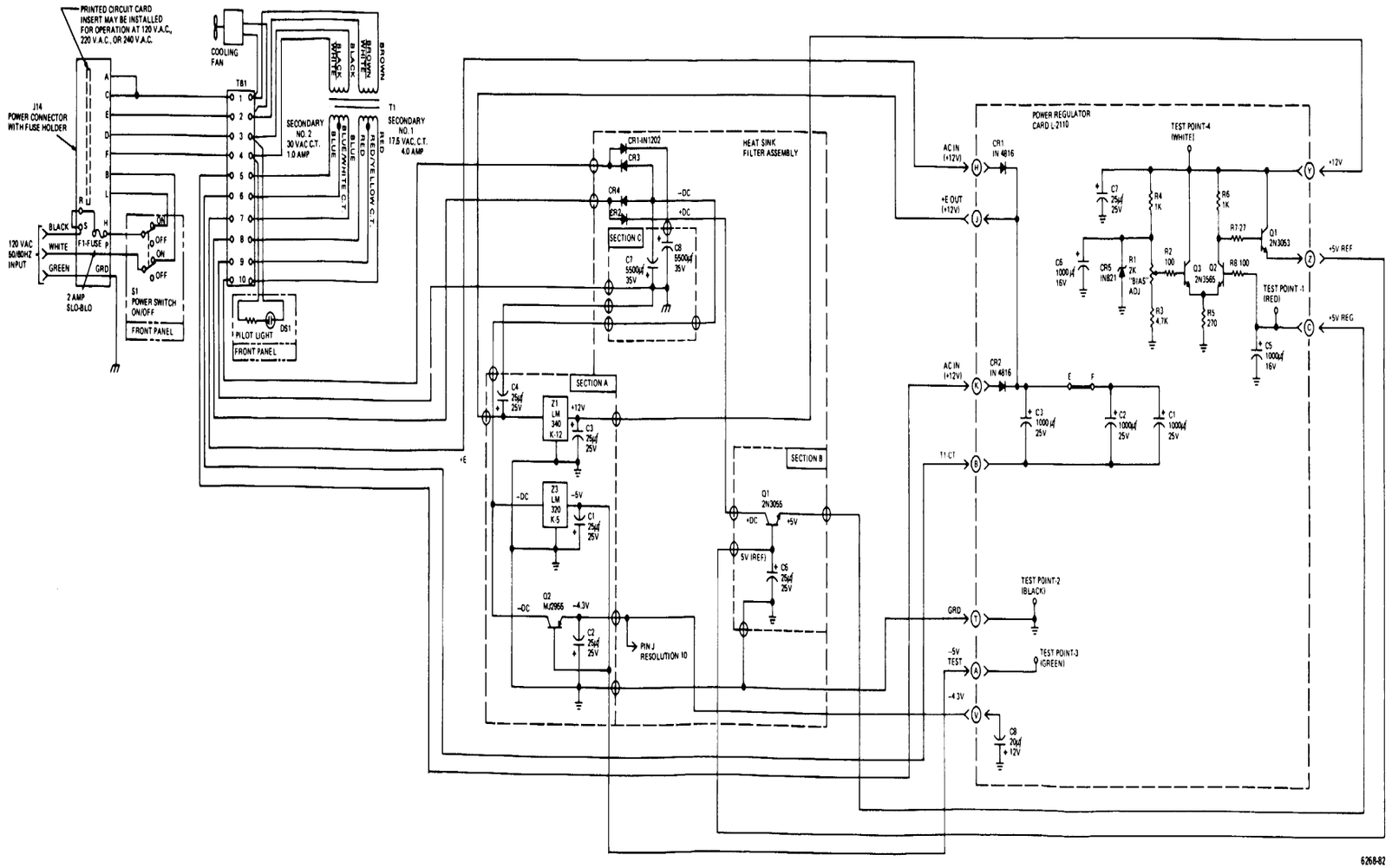


Figure FO-19. Power Regulator/Filter Assembly Schematic Diagram

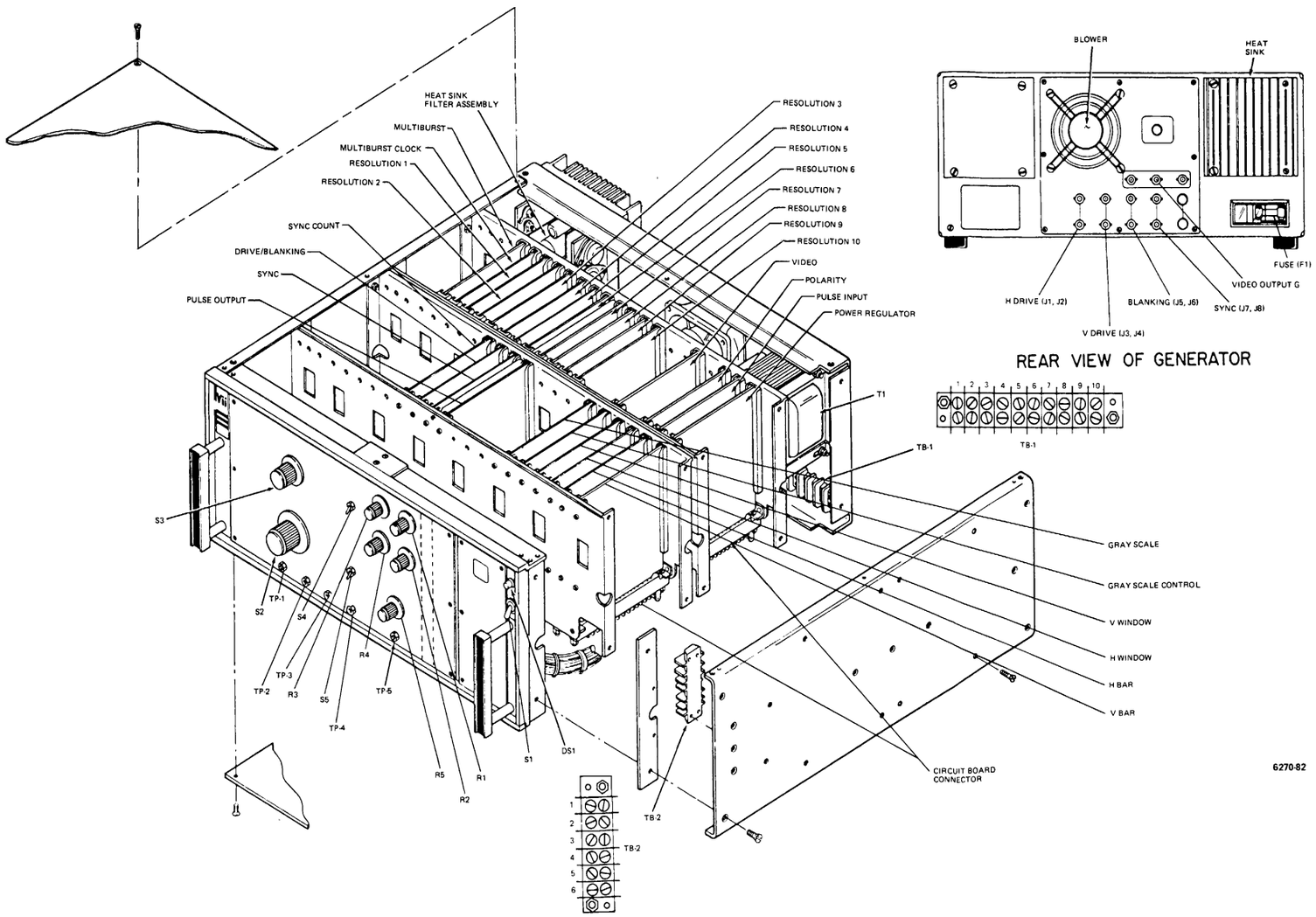


Figure FO-20. Test Pattern Generator Assembly

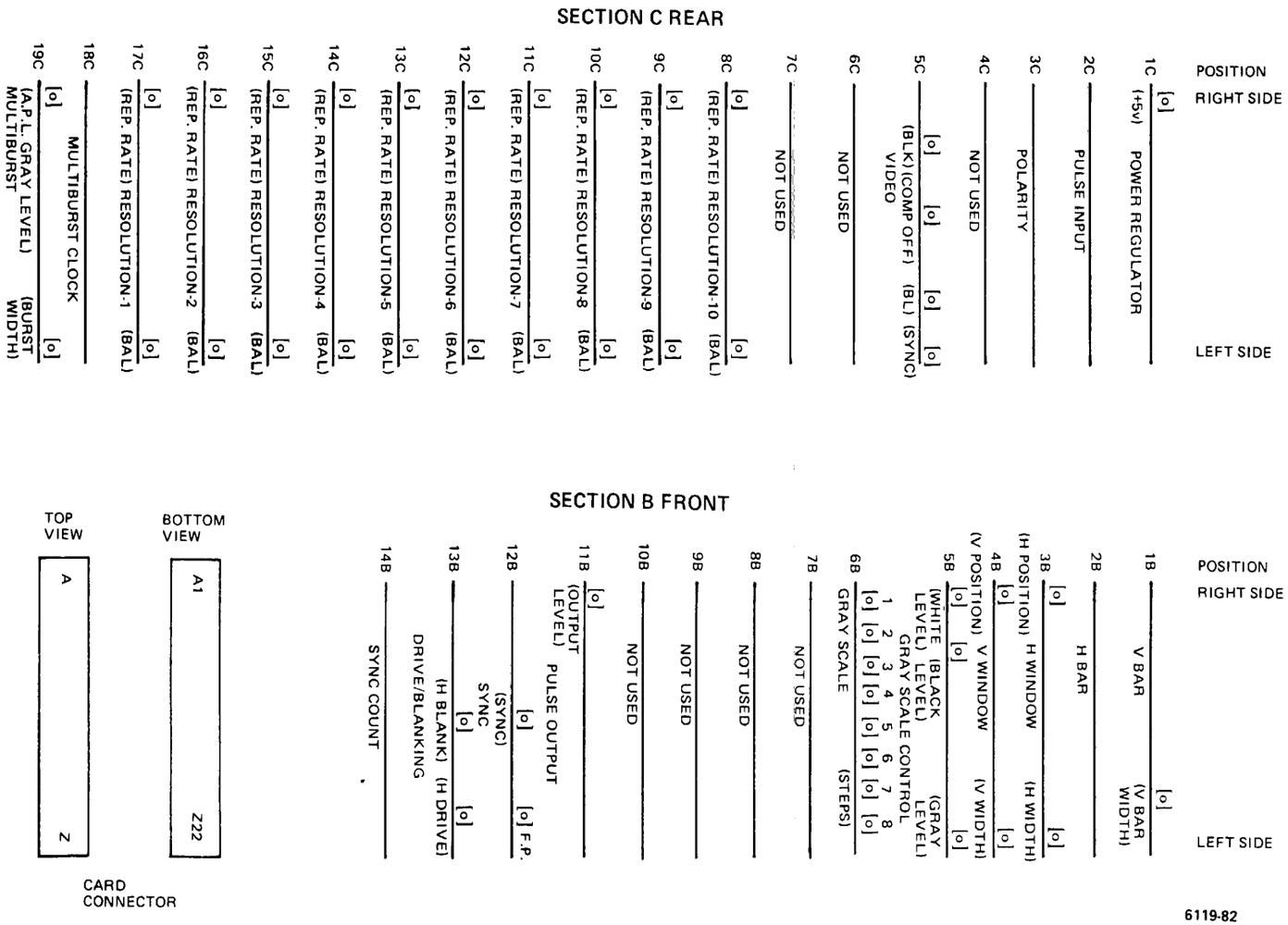


Figure FO-21. Circuit Card and Control Location

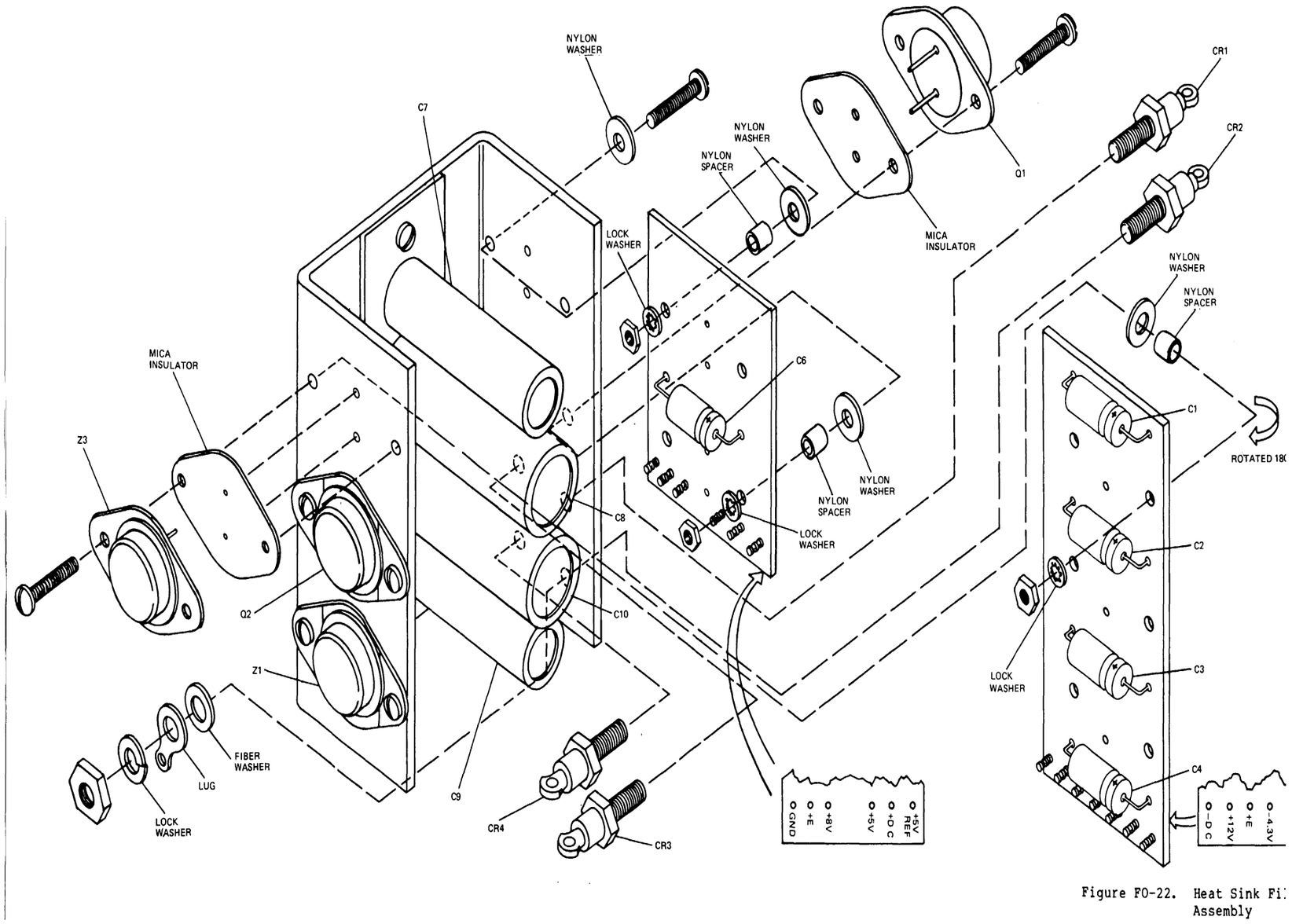


Figure FO-22. Heat Sink Fi
Assembly

Figure FO-22. Heat Sink Filter Assembly

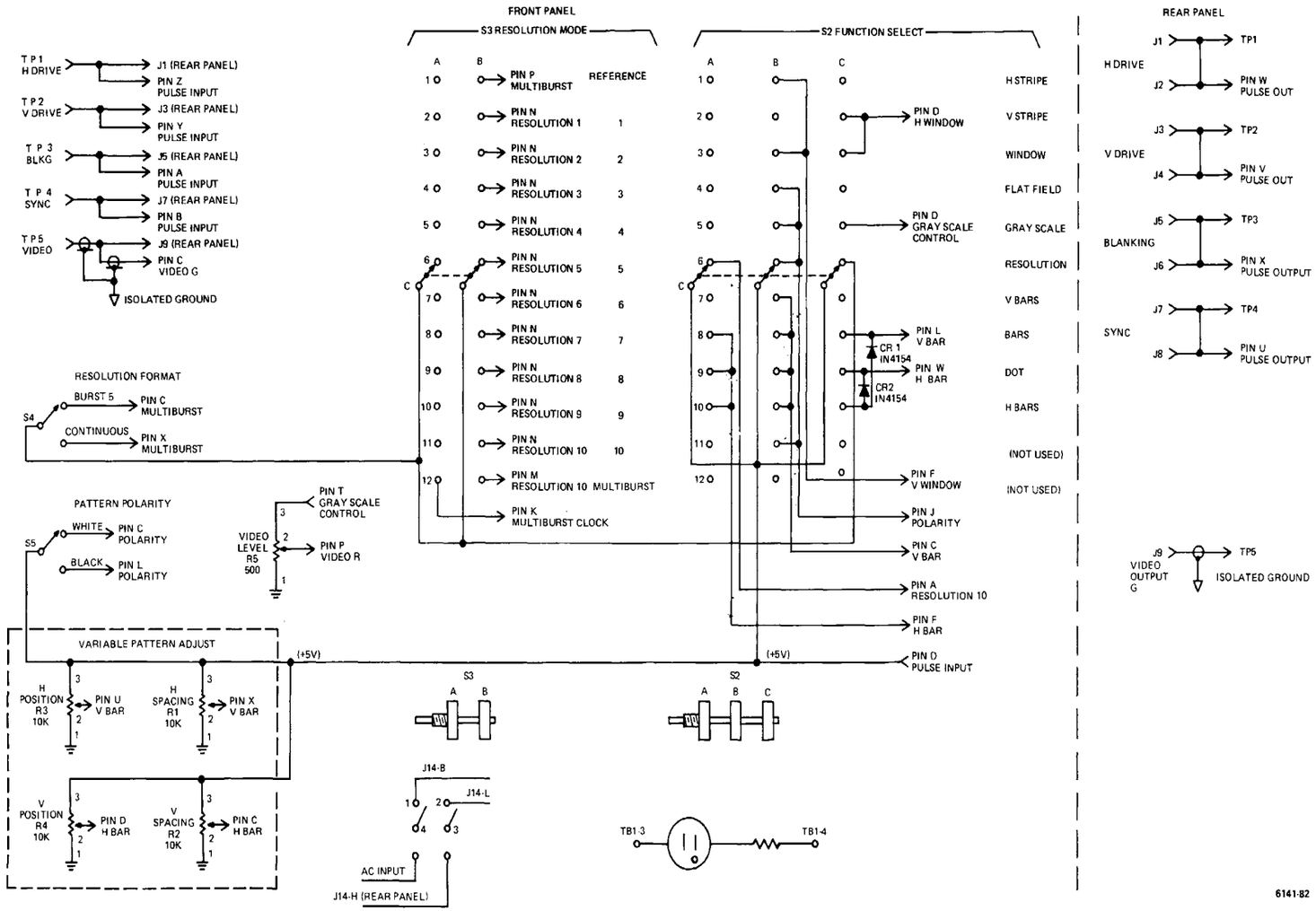


Figure FO-23. Front Panel Wiring Diagram

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